RACAL INSTRUMENTS
1260-14
DIGITAL I/O MODULE

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Before undertaking any troubleshooting, maintenance or exploratory procedure, read carefully the **WARNINGS** and **CAUTION** notices.

This equipment contains voltage hazardous to human life and safety, and is capable of inflicting personal injury.

If this instrument is to be powered from the AC line (mains) through an autotransformer, ensure the common connector is connected to the neutral (earth pole) of the power supply.

Before operating the unit, ensure the conductor (green wire) is connected to the ground (earth) conductor of the power outlet. Do not use a two-conductor extension cord or a three-prong/two-prong adapter. This will defeat the protective feature of the third conductor in the power cord.

Maintenance and calibration procedures sometimes call for operation of the unit with power applied and protective covers removed. Read the procedures and heed warnings to avoid “live” circuit points.

Before operating this instrument:

1. Ensure the proper fuse is in place for the power source to operate.

2. Ensure all other devices connected to or in proximity to this instrument are properly grounded or connected to the protective third-wire earth ground.

If the instrument:

- fails to operate satisfactorily
- shows visible damage
- has been stored under unfavorable conditions
- has sustained stress

Do not operate until, performance is checked by qualified personnel.

Racal Instruments

EC Declaration of Conformity

We

Racal Instruments Inc.
4 Goodyear Street
Irvine, CA 92718

declare under sole responsibility that the

1260-14 Digital I/O Module, P/N 404916
1260-14 (CMOS) Digital I/O Module, P/N 404916-001

They conform to the following Product Specifications:

Safety: EN61010-1:1993+A2:1995

EMC: EN61326:1997+A1:1998

Supplementary Information:

The above specifications are met when the product is installed in a Racal Instruments certified mainframe with faceplates installed over all unused slots, as applicable

The product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC (modified by 93/68/EEC).

Irvine, CA, May 9, 2002 Karen L. Denser
Engineering Director

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NOTE FOR SYSTEMS WITH 1260-OPT 01T

The “Module-Specific Syntax” section of this manual shows the command syntax for the 1260-01S Smart Card. If you are using the newer 1260-01T Smart Card, the commands will NOT work as shown.

Consult the 1260-01T Manual for a description of the commands which may be used with the 1260-01T Smart Card.

The channel numbers described in this manual are valid for the 1260-01T. The channel numbers continue to be used for the 1260-01T.

The syntax of the commands which use channel numbers has changed for those cards controlled by the 1260-01T.

The new syntax used to close a channel is:

CLOSE (@ <module address> (<channel>))

For example, with for a relay module whose <module address> is set to 7, closing <channel> 0 is performed with the command:

CLOSE (@ 7 (0))

Using the older 1260-01S, the command would be (as shown in this manual):

CLOSE 7.0

Many other command syntax differences exist. Please consult chapter 2 of the 1260-01T manual for a description of the commands which are available for the 1260-01T.

Communicating with a 1260-14 in Register-Based Mode with a 1260-01T

The 1260-14 modules are programmed using two basic operations. An 8-bit poke operation is used to write data from the slot 0 controller over the VXIbus backplane to a control register on the switch module. An 8-bit peek operation is used to read data from the status or identification register on the digital I/O module.

The 8-bit peeks and pokes are performed using an A24 address. The A24 address of each of the registers are based on the A24 address assigned by the Resource Manager to the 1260-01T and the module address of the 1260-14 module. This is described in the next section.

Calculating the Base VXI A24 Address of the 1260-14 Registers

The first step in communicating with the 1260-14 is determining the base A24 address for the 1260-14 module. This is computed using:

- The VXI A24 Address assigned to the 1260-01T by the Resource Manager
- The module address assigned to the 1260-14 module using a DIP switch

The 1260-14 modules are programmed using two basic operations. An 8-bit poke operation is used to write data from the slot 0 controller over the VXIbus backplane to a control register on the switch module. An 8-bit peek operation is used to read data from the status or identification register on the digital I/O module.

At system start-up, the Option-01T requests a block of memory to be allocated from the Resource Manager. This block of memory is placed in the VXI backplane A24 address space. The Resource Manager determines the base address of the block of memory, and writes this offset to the Option-01T's VXI Offset register.

This offset is used as the base address for writing to and reading from the relay modules. For example, suppose the address 204000 (hexadecimal) is assigned by the Resource Manager to the Option-01T.

Once the base address of the Option-01T has been computed, this address is used to calculate the address of each of the 1260 series switch modules. The address for each module is based on the module's address setting. The module address is selected by setting a DIP switch on the module, as described in the "Module Address Switches" section in Chapter 1 of 1260-01T manual.

The module address may be any number between 1 and 12. The base address for any relay module is calculated as:

<Base Address> = <Option-01T Base Address> + (<Module Address> * 1024) + 1

For example, if the <Option-01T Base Address> is 204000 (hex), the modules with the addresses 1 through 12 would have the base addresses as shown in the following table.

Module Address	Base A24 Address for Module (Hex)
1	204401
2	204801
3	204C01
4	205001
5	205401
6	205801
7	205C01
8	206001
9	206401
10	206801
11	206C01
12	207001

If the base address of the Option-01T is 200000 (hex), then module address 1 would begin at A24 address 200401, module 2 would begin at 200801, and so on.

1260-14 Register Description

The 1260-14 register map is shown in the table below. The <Base Address> is computed as shown in the preceding section.

Offset from <Base Address> (Hex)	Description
0	Data Register for Channels 1 - 8
2	Data Register for Channels 9-16
4	Data Register for Channels 17-24
6	Data Register for Channels 25-32
8	Data Register for Channels 33-40
A	Data Register for Channels 41-48
C	Data Register for Channels 49-56
E	Data Register for Channels 57-64
10	Data Register for Channels 64-72
12	Data Register for Channels 73-80
14	Data Register for Channels 81-88
16	Data Register for Channels 89-96
18	Enable Control Register #1
1A	Enable Control Register #2

So, for example, a 1260-14 with a module address of 2 would have a base address of 204801_{16}, and the data register for channels 89 through 96 would be at ($204801_{16} + 16_{16} = 204817_{16}$)

Each of the data registers controls 8 channels as an 8-bit port. Data written to the port will be output on the corresponding 8 channels. Data read from the port reflects the present state of the data on the corresponding 8 channels.

The least significant bit of the port is output to the lowest numbered channel. For example, the following shows the corresponding bit-to-channel assignment for channels 25 through 32.

Channel 25	Bit 0, LSB
Channel 26	Bit 1
Channel 27	Bit 2
Channel 28	Bit 3
Channel 29	Bit 4
Channel 30	Bit 5
Channel 31	Bit 6
Channel 32	Bit 7 (MSB)

So, by writing the value 25 decimal (= 19 hexadecimal = 0001 1001 binary), we set channels 29, 28, and 25 high and the remaining channels low.

Each of the ports of the 1260-14 must be enabled for written data to appear on the output pins. Data may be written to the ports without enabling the port, but the data will not be driven on the output pins until the port is enabled.

The register at offset 18 (hex) from the <Base Address> controls the first 8 ports comprising 64 digital output lines. The register at offset 1A (hex) from the <Base Address> controls the next 4 ports, comprising the highest 32 digital output lines. The bit assignment for these enable registers is shown below:

Enable Control Register #1 at offset 18_{16} from <Base Address>:

Bit 0 (LSB)	Enable Port 0 = Channels 1 - 8
Bit 1	Enable Port 1 = Channels 9 - 16
Bit 2	Enable Port 2 = Channels 17 - 24
Bit 3	Enable Port 3 = Channels 25 - 32
Bit 4	Enable Port 4 = Channels 33 - 40
Bit 5	Enable Port 5 = Channels 41 - 48
Bit 6	Enable Port 6 = Channels 49 - 56
Bit 7 (MSB)	Enable Port 7 = Channels 57 - 64

Enable Control Register #2 at offset $1A_{16}$ hex from <Base Address>

Bit 0	Enable Port 8 = Channels 65 - 72
Bit 1	Enable Port 9 = Channels 73 - 80
Bit 2	Enable Port 10 = Channels 81 - 88
Bit 3	Enable Port 11 = Channels 89 - 96

To enable a port of 8 digital output lines, write a 1 to the corresponding bit of the control register. To disable the port, write a 0 to the corresponding bit of the control register.

For example, if the value 80 decimal (= 50 hexadecimal = 0101 0000 binary) is written to control register #1 at offset 18_{16}, then channels 49 through 56, and channels 33 through 40 will be enabled, while channels 1 through 32, 41 through 48, and 57 through 64 will be disabled.

Note that when a channel is enabled, the data written to the channel will be the same as that read from the channel (unless external circuitry prevents driving the channel high or low).

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Chapter 1

MODULE SPECIFICATION

General

The 1260-14 provides 96 TTL or CMOS compatible digital I/O lines in twelve groups of 8 bits each. Each group of 8 bits (hereafter referred to as a port), can be read from or written to asynchronously using the commands READ and WRITE. Additionally, up to 12 ports may be grouped together and synchronously operated using an external clock for as many as 256 consecutive operations by using the appropriate SETUP commands. The last data previously written to or read from a port may be retrieved by using the PDATAOUT command. The current state of the 1260-14 may be determined by using the PSETUP command. Refer to the individual syntax descriptions for each command, as well as the examples given later for the specifics regarding these operations.

Two handshake lines are available for the synchronous I/O mode of operation that can operate at a transfer rate of up to 1 kHz. See Page 3-2 for a description of the synchronous mode handshake.

Tri-state control is provided for each port, and may be manipulated by either hardware, software or both. The software tri-state control will force all ports to tri-state following a power-on or reset. See Page 3-4 for a description of the tri-state controls.

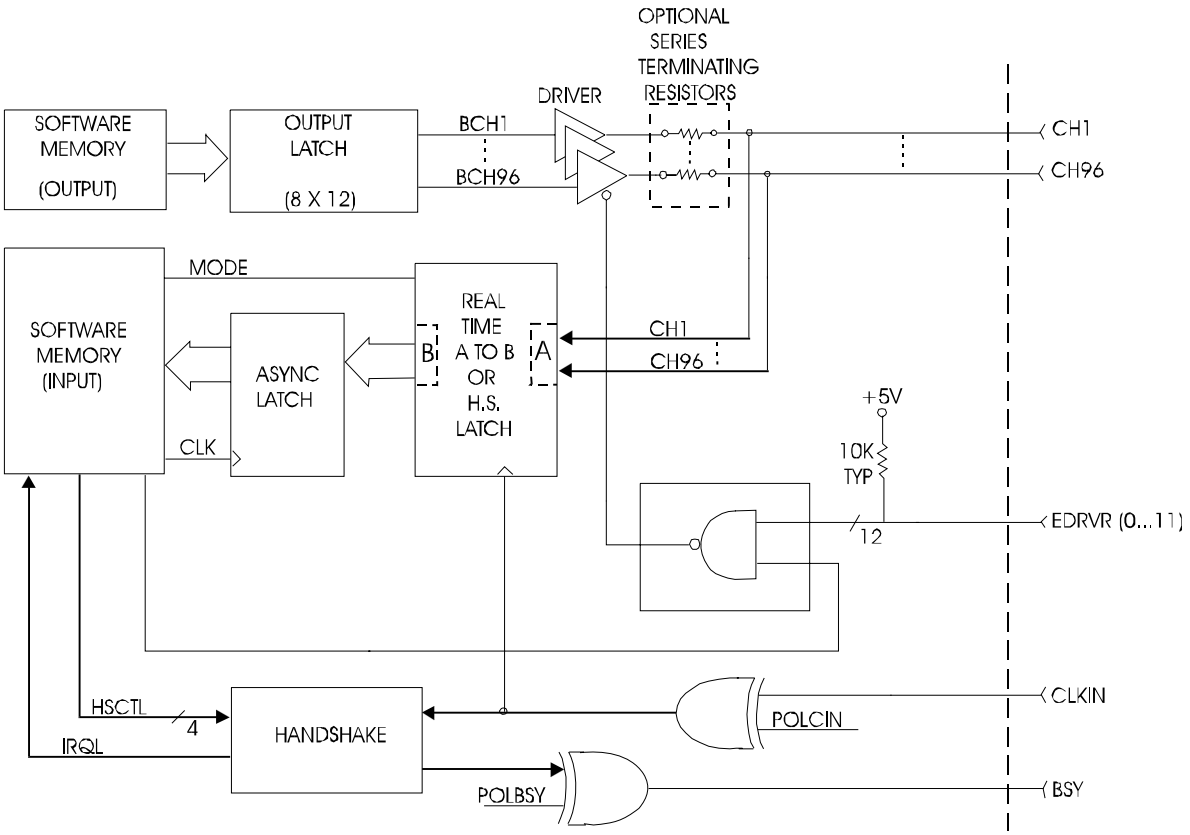

Figure 1-1, 1260-14 Block Diagram

Module Specification

User Connector	Two 50-pin IDC and two 60-pin IDC	
Number of I/O Channels	96 Channels	
Configuration	I/O lines selected as either input or output on an 8-bit byte basis	
Data Rate	Static to approximately 1 kHz	
Operating Modes	Asynchronous Synchronous	
Input/Output	TTL or CMOS (Option 14) compatible	
Output Voltage	TTL	CMOS
V_{out} (High)	$\geq$2.4 V at -15 mA	>3.8 V at 6mA
V_{out} (Low)	$\leq$0.5 V at 48 mA	<0.4 V at 6mA

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Input Voltage		
V_{in} (High)	$\geq$2.0 V	$\geq$3.15 V
V_{in} (Low)	$\leq$0.8 V	$\leq$0.9 V
V_{ih} (Max)	5.25 V	5.00 V
Cooling Requirement		
Airflow	1.2 liters/sec	
Backpressure	0.6 mm of H_20	
Power Requirement (I_{pm})		
+5V	2.38A (4.78A with Option 01)	
Weight	2.69 lbs (1.21 kg)	
	2.97 lbs (1.34 kg with Option 01)	
Minimum Option 01 Firmware		
Revision	17.1	

* An Open Collector version of the 1260-14 is also available.

CAUTION:

Damage to the Digital I/O card or the user's equipment could occur if the user write-enables the output driver for a port that is connected to a device that is also attempting to drive the data lines.

Pin Configuration

The 1260-14 Digital I/O module has 96 channels, grouped as twelve 8-bit ports available at front panel connectors J1 through J4. Each port may be configured as an input or an output.

Refer to **Figure 1-2** for the pin configurations of the 50 and 60-pin connectors on the front panel, and to **Table 1-1** for correspondence between the physical channel assignments and the port numbers used in the command codes.

Refer to **Table 1-2** for correspondence between the front panel pins and the signal names and descriptions.

Table 1-1, 1260-14 Channels and Ports

Channel No.	Port No.	Tri-State Control
1 - 8	0	EDRVR0
9 - 16	1	EDRVR1
17 - 24	2	EDRVR2
25 - 32	3	EDRVR3
33 - 40	4	EDRVR4
41 - 48	5	EDRVR5
49 - 56	6	EDRVR6
57 - 64	7	EDRVR7
65 - 72	8	EDRVR8
73 - 80	9	EDRVR9
81 - 88	10	EDRVR10
89 - 96	11	EDRVR11

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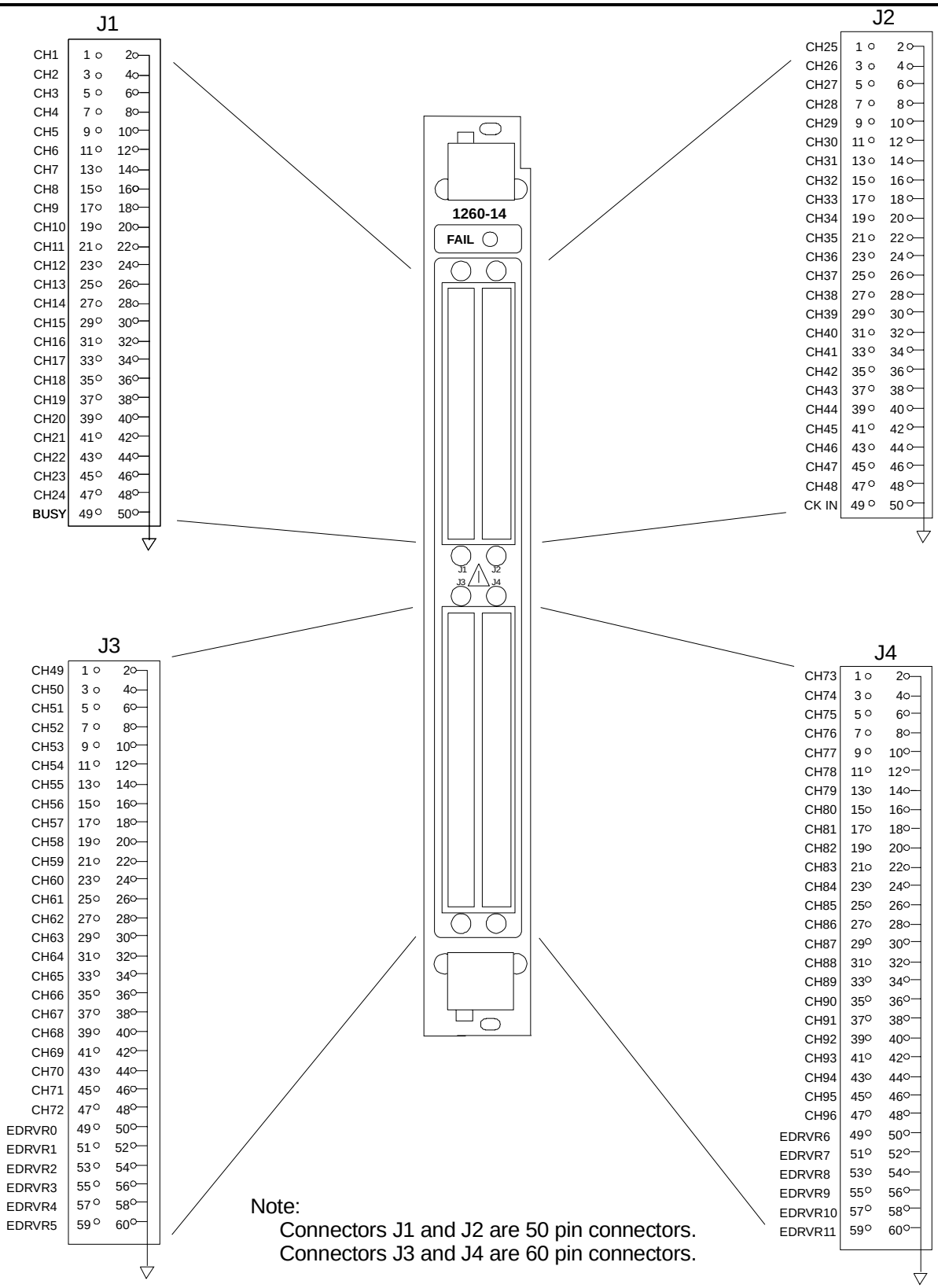

Figure 1-2, 1260-14 Front Panel and Pin Configuration

Table 1-2, 1260-14 Pins, Signals and Descriptions

J1 Pin	Row A Signal	Signal Description
1	CH1	Channel 1 I/O
3	CH2	Channel 2 I/O
5	CH3	Channel 3 I/O
7	CH4	Channel 4 I/O
.	.	.
.	.	.
.	.	.
45	CH23	Channel 23 I/O
47	CH24	Channel 24 I/O
49	BSY	BUSY Handshake output

J1 Pin	Row B Signal	Signal Description
2	GND	Channel 1 RTN
4	GND	Channel 2 RTN
6	GND	Channel 3 RTN
8	GND	Channel 4 RTN
.	.	.
.	.	.
.	.	.
44	GND	Channel 22 RTN
46	GND	Channel 23 RTN
48	GND	Channel 24 RTN
50	GND	BUSY Signal return

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Table 1-2, 1260-14 Pins, Signals and Descriptions (continued)

J2 Pin	Row A Signal	Signal Description
1	CH25	Channel 25 I/O
3	CH26	Channel 26 I/O
5	CH27	Channel 27 I/O
7	CH28	Channel 28 I/O
.	.	.
.	.	.
.	.	.
45	CH47	Channel 47 I/O
47	CH48	Channel 48 I/O
49	CLKIN	CLKIN Handshake input

J2 Pin	Row B Signal	Signal Description
2	GND	Channel 25 RTN
4	GND	Channel 26 RTN
6	GND	Channel 27 RTN
8	GND	Channel 28 RTN
.	.	.
.	.	.
.	.	.
44	GND	Channel 46 RTN
46	GND	Channel 47 RTN
48	GND	Channel 48 RTN
50	GND	CLKIN Signal return

Table 1-2, 1260-14 Pins, Signals and Descriptions (continued)

J3 Pin	Row A Signal	Signal Description
1	CH49	Channel 49 I/O
3	CH50	Channel 50 I/O
5	CH51	Channel 51 I/O
7	CH52	Channel 52 I/O
.	.	.
.	.	.
.	.	.
45	CH71	Channel 71 I/O
47	CH72	Channel 72 I/O
49	EDRVR 0	Driver Enable 0
51	EDRVR 1	Driver Enable 1
53	EDRVR 2	Driver Enable 2
55	EDRVR 3	Driver Enable 3
57	EDRVR 4	Driver Enable 4
59	EDRVR 5	Driver Enable 5

J3 Pin	Row B Signal	Signal Description
2	GND	Channel 49 RTN
4	GND	Channel 50 RTN
6	GND	Channel 51 RTN
8	GND	Channel 52 RTN
.	.	.
.	.	.
.	.	.
44	GND	Channel 70 RTN
46	GND	Channel 71 RTN
48	GND	Channel 72 RTN
50	GND	EDRVR0 RTN
52	GND	EDRVR1 RTN
54	GND	EDRVR2 RTN
56	GND	EDRVR3 RTN
58	GND	EDRVR4 RTN
60	GND	EDRVR5 RTN

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Table 1-2, 1260-14 Pins, Signals and Descriptions (continued)

J4 Pin	Row A Signal	Signal Description
1	CH73	Channel 73 I/O
3	CH74	Channel 74 I/O
5	CH75	Channel 75 I/O
7	CH76	Channel 76 I/O
.	.	.
.	.	.
.	.	.
45	CH95	Channel 95 I/O
47	CH96	Channel 96 I/O
49	EDRVR6	Driver Enable 6
51	EDRVR7	Driver Enable 7
53	EDRVR8	Driver Enable 8
55	EDRVR9	Driver Enable 9
57	EDRVR10	Driver Enable 10
59	EDRVR11	Driver Enable 11

J4 Pin	Row B Signal	Signal Description
2	GND	Channel 73 RTN
4	GND	Channel 74 RTN
6	GND	Channel 75 RTN
8	GND	Channel 76 RTN
.	.	.
.	.	.
.	.	.
44	GND	Channel 94 RTN
46	GND	Channel 95 RTN
48	GND	Channel 96 RTN
50	GND	EDRVR6 RTN
52	GND	EDRVR7 RTN
54	GND	EDRVR8 RTN
56	GND	EDRVR9 RTN
58	GND	EDRVR10 RTN
60	GND	EDRVR11 RTN

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Chapter 2

INSTALLATION INSTRUCTIONS

Unpacking and Inspection

1. Remove the 1260-14 module and inspect it for damage. If any damage is apparent, inform the carrier immediately. Retain shipping carton and packing material for the carrier's inspection.

2. Verify that the pieces in the package you received contain the correct 1260-14 module option and the 1260-14 Users Manual. Notify EADS North America Defense Test and Services, Inc. if the module appears damaged in any way. Do not attempt to install a damaged module into a VXI chassis.

3. The 1260-14 module is shipped in an anti-static bag to prevent electrostatic damage to the module. Do not remove the module from the anti-static bag unless it is in a static-controlled area.

CAUTION:

Proper ESD handling procedures must always be used when packing, unpacking or installing any 1260 series cards. Failure to do so may cause damage to the unit.

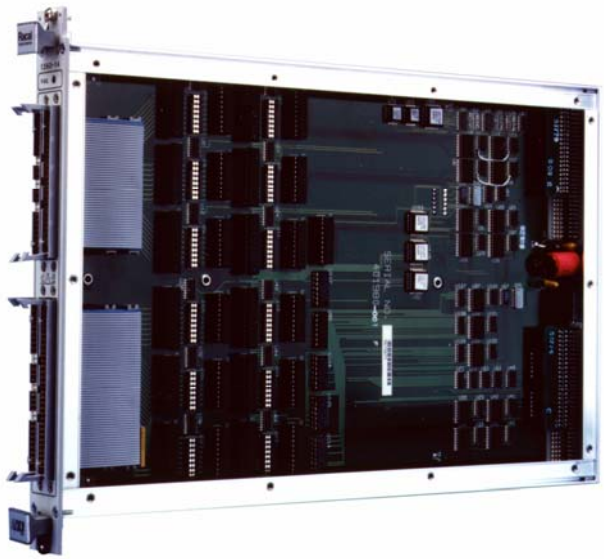

Figure 2-1, 1260-14

Reshipment Instructions

1. Use the original packing when returning the switching module to EADS North America Defense Test and Services, Inc. for calibration or servicing. The original shipping carton and the instrument's plastic foam will provide the necessary support for safe reshipment.

2. If the original packing material is unavailable, wrap the switching module in an ESD Shielding bag and use plastic spray foam to surround and protect the instrument.

3. Reship in either the original or a new shipping carton.

Option 01 Installation

Installation of the Option 01 to the 1260-14 is described in the Installation section of the 1260 Series VXI Switching Cards Manual (RII P/N 980673-999).

Module Installation

Installation of the 1260-14 Digital I/O Module into a VXIbus mainframe, including the setting of DIP switches, is described in the Installation section of the 1260 Series VXI Switching Cards Manual. The ID byte DIP switches, SW1-5 and SW1-6, should be set OFF (RII P/N 980673-999).

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Chapter 3

MODULE SPECIFIC SYNTAX

Asynchronous and Synchronous Modes of Operation

Each port on the 1260-14 can operate in either an asynchronous or a synchronous mode. The number of synchronous mode ports may be modified using the SETUP SYNC command. The default after power-up or reset is for all ports to be in the asynchronous mode. The current operating mode of the ports may be determined at any time with the PSETUP command. See the syntax description of the PSETUP and SETUP SYNC commands for details and examples.

Asynchronous Mode

The asynchronous mode allows data to be read from or written to a port in response to a READ or WRITE command. The following restrictions apply to all asynchronous operations:

Those ports defined as asynchronous cannot participate in synchronous operations.

Asynchronous commands are not allowed on any port while synchronous operations are armed and waiting for clocks.

Asynchronous WRITE commands are valid on synchronous write ports to allow the port to be preset to a starting value. Asynchronous READ commands are not allowed on synchronous read ports.

Synchronous Mode

The synchronous mode of operation allows data to be read from or written to a port in response to a clock edge. Typically, this is done by:

1. Defining the test parameters and data via the various SETUP commands.

2. Arming the test via the SETUP <address>.ARM ON command.

3. Applying a series of TTL clock inputs to the CLKIN line until the last operation on all ports has been completed, causing the test to automatically disarm. It is also possible to manually disarm the test before it has completed all of the test vectors. This is done via the SETUP <address>.ARM OFF command.

4. Reading back the results using the PDATAOUT command.

The following restrictions apply to all synchronous operations:

Synchronous ports are always grouped together and are always the lowest numbered ports; i.e., the first synchronous port is always port 0, and the second is always port 1, etc.

All ports not specified as synchronous are asynchronous by default.

A port may read or write during synchronous operations, but not both.

Once a synchronous test has been set up, it must be armed before the unit will enable the handshake lines.

Synchronous operations may not be set up once the 1260-14 is armed.

There is a maximum of 256 synchronous operations (referred to as vectors) per port.

All synchronous ports are clocked simultaneously; i.e., if 5 synchronous ports are defined, the first active edge of the clock will cause the appropriate action to occur on all five ports.

Synchronous ports will support the asynchronous WRITE command, but will not support the asynchronous READ command.

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Synchronous Mode Handshaking

The module has a two line handshake available for use in the synchronous mode. The first is the BUSY line which is set by the 1260-14 when it is busy processing, and the second is the CLKIN line which the user toggles to clock the next synchronous operation. The user may specify the polarity of the BUSY line and the active edge of the CLKIN line by using the appropriate SETUP command. Refer to **Figure 3-1** for the timing diagrams of the input and output handshaking modes available. Both the BUSY and CLKIN lines are valid only when a synchronous operation is defined and armed.

NOTE:

Both the BUSY and the CLKIN lines are valid only when synchronous operations are defined and armed. Changes on the CLKIN line will be ignored by the 1260-14 when the card is not armed. Spurious outputs on the BUSY line should also be ignored unless the unit is armed.

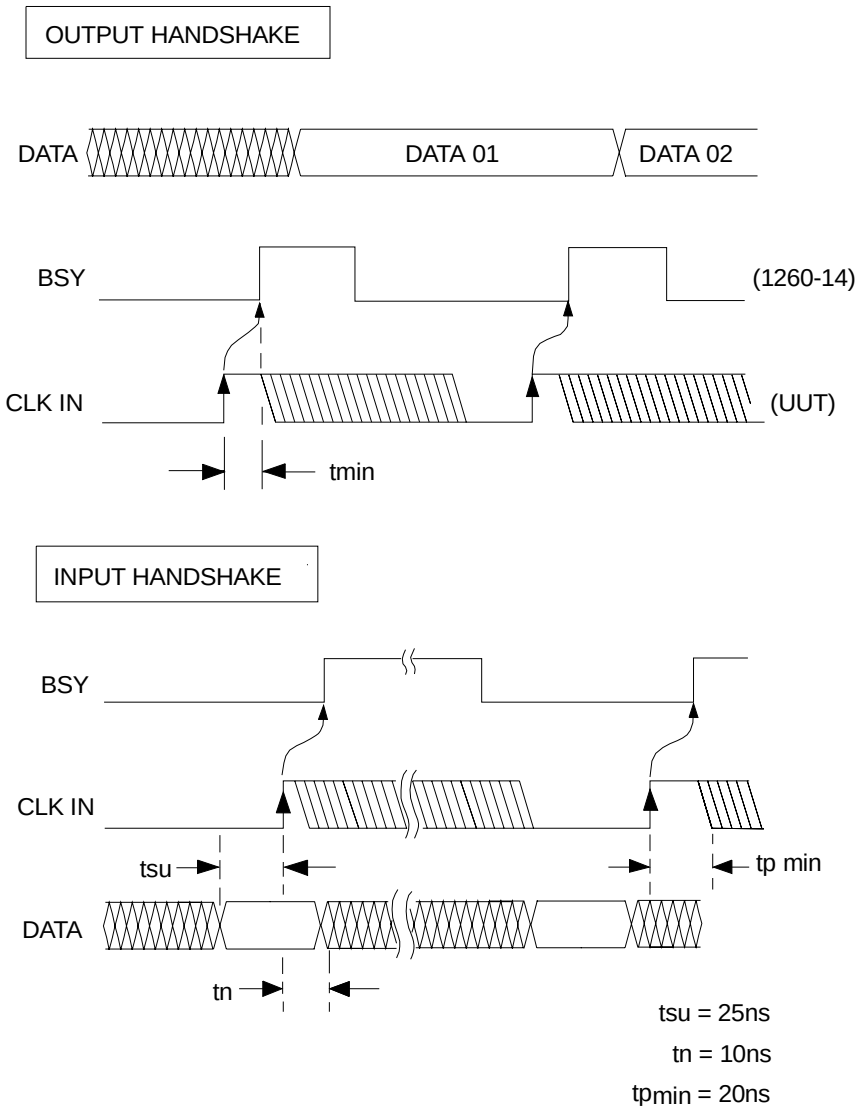

Figure 3-1, 1260-14 Input and Output Handshake Modes

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Tri-State Control

Each port on the 1260-14 may be either tri-stated or write-enabled. This may be controlled by either hardware, software or both. In hardware, each port has an Enable Driver line (EDRVR 0-11) that is tied to a logic high via an internal pull-up resistor. This allows the software to either tri-state or write-enable the port's driver when requested via the SETUP ENABLE command. The user may override this at any time and force a port to the tri-state condition by connecting a logic low to the appropriate EDRVR line. See **Table 3-1** for a detailed definition of this relationship. See **Figure 3-2** for a block diagram of the tri-state control mechanism.

Table 3-1, Tri-state Control Truth Table

EDRVR State	Software Enable	Port Status
High	True	Write Enabled
Low	True	Tri-stated
High	False	Tri-stated
Low	False	Tri-stated

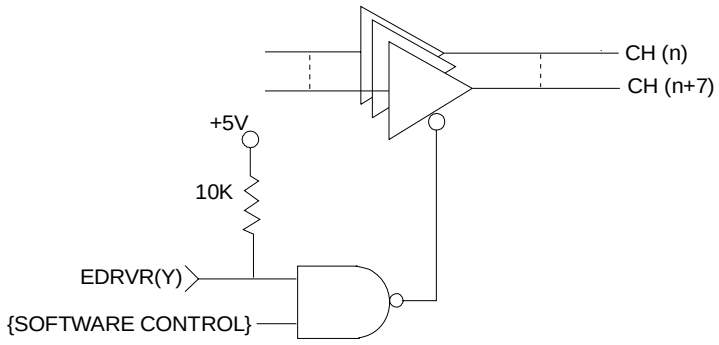

Figure 3-2, 1260-14 Tri-State Control

Module Specific Syntax

The 1260-14 Digital I/O module supports the PDATAOUT, PSETUP, READ, RESET, SETUP, and WRITE commands. The general form of the module specific syntax for the 1260-14 Digital I/O module is:

command address.parameters

where:

command is one of the 1260-14 module specific commands.

address is the module address set by SW1 on the 1260-14 (1-12).

parameters are the command specific parameters and data.

NOTE:

The address used here is <u>not</u> the VXIbus defined logical address of the Master. It is a designation unique to the 1260 Series and is used by the 1260 Option 01 to identify individual 1260 modules. This switch setting is a requirement since a single Option 01 can control multiple 1260 Series modules. This address corresponds to the binary value of the switch setting of SW1 on the switching module PCB, and can take on the values from 1 to 12.

Syntax Notations and Conventions

The following syntax notations and conventions are used throughout the manual:

All terms in upper case letters are used directly in the command syntax, although case is not important in the actual command string sent to the Option 01.

All items in brackets ([ ]) are optional.

All lower case letters within greater/less than pairs (< >) are to be replaced by a numeric value, as specified in the syntax description.

A vertical bar (|) represents the "or" function, and specifies that the user must select one and only one of the items separated by bars.

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All lines must be terminated by an ASCII line feed <LF>, EOI or both.

Write data may be in either decimal, hexadecimal, or binary format. Non-decimal numbers must be preceded with "H" for hex or "B" for binary.

Definition of Commands

PDATAOUT command

Syntax: PD[ATAOUT] <address>[.<ports>][,<address>[.<ports>],...]

<address>::= Module address of the 1260-14 (1-12)

<ports>::= One or more consecutive ports to return data from. A single port is specified as a decimal number from 0 to 11. A group of ports is specified as two decimal numbers from 0 to 11 separated by a hyphen, (-), with the lower numbered port to the left and the higher numbered port to the right. For example, the command string PD 1.3-5 would return values for ports 3, 4 and 5.

Description: The PDATAOUT command will cause the module specified by the logical address to return the data associated with each requested port. The format of the return data is as follows:

<address>. 1260-14 DIGITAL INPUT/OUTPUT MODULE <CR><LF>

<address>. [<port>: <data>,...]<CR><LF>

<address>.END<CR><LF>

where:

<address>::= A three digit module address. (001-012)

<data>::= From 0 to 256 pieces of data in either decimal, hexadecimal or binary format.

<port>::= A 2-digit number specifying the port to associate with the data that follows.

NOTE:

There is a space following the period on each line except for the line containing the END string. This allows the user to detect when the last line of a multiple line reply has occurred by looking at the fifth character of each line to see if it is a space or an ASCII "E". This convention is true for all commands returning multiple line outputs.

Output data for the specified modules and ports are in the same order as requested in the command. Each port's data is preceded with the port number and a colon. The type and format of the data returned will depend on how the port is defined and the last operation performed on the port. This is determined as follows:

If the port is defined as a synchronous mode read port, the command will return the data from the most recent synchronous test, using the same data width and format that was specified when the test was defined. If the port has been defined as synchronous but no test has been run since the port was defined, no values are returned (e.g, "001. 07:").

If the port is defined as a synchronous mode write port, the command will return the most recent write data loaded for this port, using the same data width and format used to load the data. If no data is loaded, no values are returned (e.g., "001. 07:").

If the port is defined as an asynchronous port, the command will return the results of the most recent READ or WRITE command, using the same data width and format used in that command. If no READ or WRITE commands have been sent, no values are returned (e.g., "001. 07:").

Example:

Assume that port 0 is a synchronous mode byte-wide (8-bit) port that read in the hex values 9f, 7f, 3f and 1f during vectors 1-4 of the last synchronous test. Port 1 is a synchronous mode byte wide port that wrote out the decimal values 21, 31, 41 and 51 during vectors 1-4 during the last synchronous test. Port 2, along with port 3, is an asynchronous word-wide (16-bit) port that was last used to read a hex 7AA6. Port 4 is an asynchronous byte wide port that was last used to write a binary 10101101. The command:

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would return the following data:

001. 1260-14 DIGITAL INPUT/OUTPUT MODULE<CR><LF>
001. 00:9F,7F,3F,1F<CR><LF>
001. 01:21,31,41,51<CR><LF>
001. 02:7AA6<CR><LF>
001. 04:10101101<CR><LF>
001.END<CR><LF>

PSETUP command

Syntax: PS[ETUP] <address>

<address>::= Module address of the 1260-14 (1-12)

Description: This command will cause the module to return the condition of all the setup variables for the 1260-14 at the specified module address. The following is a sample output from a PSETUP command for a 1260-14 at module address 1, showing the power-up default condition for the setup variables:

001. 1260-14 DIGITAL INPUT/OUTPUT MODULE

001. ENABLE
001. SYNC 0
001. BUSY POS
001. CLKIN POS
001. ARM OFF
001.END

READ command

Syntax:

Byte: READ <address>.<ports>[,Y][,B | ,H]
Word: READ <address>.<ports>,W[,B | ,H]
Bit: READ <address>.<ports>,X<bit>[,X<bit>...]
Fast: READ <address>.<ports>,Z,[,H]

<address>::= Module address of the 1260-14 (1-12)

<ports>::= One or more consecutive ports to read from. A single port is specified as a decimal number from 0 to 11. A group of ports is specified as two decimal numbers from 0 to 11 separated by a hyphen, (-), with the least significant port to the right and the most significant port to the left. For example, the command READ 1.3-5,Y would return values for ports 3, 4 and 5.

<bit>::= The individual bit number (0-7) to read in the bit mode. The user may specify multiple bits by separating each

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X<bit> with commas. Bit 0 is the LSB and bit 7 the MSB.

A "B" specifies that the output format for the data is binary. Note that this format is unavailable in the fast byte mode to keep the output on a single 80-character line.

An "H" specifies that the output format for the data is hexadecimal.

A "Y" causes a byte-wide (8-bit) read of the port. This is the default if no width is specified. See Example 1 above for a sample of a byte-wide READ command.

A "W" causes a word-wide (16-bit) read of a pair of ports. Word-wide operations are specified on even-numbered ports only, and read the least significant 8 bits from the even port and the most significant 8 bits from the following odd-numbered port.

Description: This command performs an asynchronous read from a single port or a group of consecutive ports. No handshaking is required for this operation. This command will only read those ports defined as asynchronous ports. It will not read from a synchronous port. A read from a write-enabled port will return the value that the port is currently driving. As soon as the command is received, an immediate read of the specified port(s) occurs. The data for each requested port is sent to the user in the order of lowest to highest port, and with the exception of the fast mode, data is returned in a form identical to that of a PDATAOUT.

Read operations may be performed as either a bit, byte or word wide operation, with byte-wide being the default. In addition, on firmware revisions 18.1 and beyond, there is a byte-wide fast output mode available that reduces the output string size, significantly cutting down on the data transfer time from the 1260 Option 01 to the Slot 0 controller. Data is formatted in either decimal, hexadecimal or binary with the default being decimal. The width and format of the output are specified as follows:

Example 1:

Assume that ports 5-11 are defined as asynchronous and are tri-stated, port 5 is sensing a 23, port 6 is sensing a 0, port 7 is sensing 127 and the user sends the following command:

READ 1.5-7,Y

The user would read back:

001. 1260-14 DIGITAL INPUT/OUTPUT MODULE<CR>

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<LF>

001. 05: 23<CR><LF>
001. 06: 0<CR><LF>
001. 07: 127<CR><LF>
001.END<CR><LF>

Example 2:

Assume that all ports are defined as asynchronous and are tri-stated, port 0 is sensing a hex 1e, port 1 is sensing a hex c7, port 2 is sensing a hex d3, port 3 is sensing a hex a0 and the user sends the following command:

READ 1.0-2,W,H

The user would read back:

001. 1260-14 DIGITAL INPUT/OUTPUT MODULE<CR><LF>

001. 00: C71E<CR><LF>
001. 02: A0D3<CR><LF>
001.END<CR><LF>

An "X" causes a bit-wide read of the port. Any combination of the 8 bits from X0-X7 may be read simultaneously. The output will contain the status of each bit in binary format and in the same order as specified in the command.

Example 3:

Assume that ports 7-11 are defined as asynchronous and are tri-stated, port 7 is sensing a binary 10001010, port 8 is sensing a 01111101, and the user sends the following command:

READ 1.7-8,X7,X3,X1,X0

The user would read back:

001. 1260-14 DIGITAL INPUT/OUTPUT MODULE<CR><LF>

001. 07: 1110<CR><LF>
001. 08: 0101<CR><LF>
001.END<CR><LF>

A "Z" causes a byte-wide (8 bit) read of the port, but instead of using the PDATAOUT format for returning the data, it uses a shorter single line output to reduce the amount of time needed to

transfer the read data. It is identical to the standard byte width read with the exception that binary formatting is not available, and the output contains no header line, END line, module address or port numbers. All the output line contains is the port data separated by commas. Data is returned in least significant port to most significant port order. This type of read is only available on firmware revisions 18.1 or later.

Example 4:

Assume that ports 5-11 are defined as asynchronous and are tri-stated, port 5 is sensing a hex 7f, port 6 is sensing a hex 01, port 7 is sensing a hex c3 and the user sends the following command:

READ 1.5-7,Z,H

The user would read back:

7F,01,C3<CR><LF>

RESET command

Syntax: RES[ET]

Description: The RESET command resets the 1260-14 card to the power-up state. Specifically, the following attributes are programmed after the RESET command is executed:

BUSY Polarity	Positive
CLKIN Polarity	Positive
Synchronous Ports	None (SYNC 0)
Arm	Off
All Ports	Tri-stated

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SETUP ARM command

Syntax: SE[TUP] <address>.AR[M],ON | OFF

<address>::= Module address of the 1260-14 (1-12)

Description: This command is used to arm and disarm the synchronous handshake mode. Setup data may only be modified while ARM is OFF. Synchronous data transfers may only take place when ARM is ON. Once the card is armed, any attempts to send a setup command other than a SETUP <address>.ARM,OFF will cause an error.

The completion of the last synchronous READ/WRITE operation in a test automatically sets the ARM mode to OFF. The CLKIN signal used to cause data transfers is ignored as long as ARM is OFF.

Each time the ARM is set to ON, synchronous READ/WRITE operations restart at the first location in the port's buffer. This means that if the user sets up a port to output five data items, resetting the ARM causes the first data item to be transferred at the next occurrence of the CLKIN signal. This is regardless of where in the buffer the test had been when the ARM was set to OFF. PDATAOUT commands are not recognized until ARM is OFF. The default power-up condition of ARM is OFF.

Example:

This command sets ARM mode to ON within the module at address 1.

```
SETUP 1.ARM,ON
```

SETUP BUSY command

Syntax: SE[TUP] <address>.BU[SY],POS | NEG

<address>::= Module address of the 1260-14 (1-12)

Description: This command defines the polarity of the BUSY handshake line. Setting the polarity to POS causes the BUSY line to be set HIGH when the 1260-14 is busy processing during synchronous operation. Setting the polarity to NEG causes the BUSY line to be set LOW when the module is busy. The default power-up condition is POS.

NOTE:

The BUSY line is only valid when synchronous operations are defined and armed. Spurious signals at other times should be ignored by the user.

Example:

This command sets the polarity of the BUSY signal to negative within the module at address 2.

SETUP 2.BUSY,NEG

SETUP CLKIN command

Syntax: SE[TUP] <address>.CL[KIN],POS | NEG

<address>::= Module address of the 1260-14 (1-12)

Description: This command defines the active edge of the CLKIN handshake signal. Setting CLKIN to POS causes the module to trigger on the positive (or rising) edge of the CLKIN signal. Setting the polarity to NEG causes the module to trigger on the negative (or falling) edge of the CLKIN signal. The default power-up condition is POS.

NOTE:

The CLKIN line is only monitored when synchronous operations are defined and armed. Spurious signals at other times will be ignored.

Example:

This command sets the active edge of the CLKIN signal to negative within the module at address 3.

SETUP 3.CLKIN, NEG

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SETUP ENABLE command

Syntax: SE[TUP] <address>.EN[ABLE][,<ports>,<ports>,...]

<address>::= Module address of the 1260-14 (1-12)

<ports>::= One or more consecutive ports to write to. A single port is specified as a decimal number from 0 to 11. A group of ports is specified as two decimal numbers from 0 to 11 separated by a hyphen, (-), with the lower numbered port to the left and the higher numbered port to the right. For example, the command SE 1.EN,3-5 would write-enable ports 3, 4 and 5.

Description: This command write-enables the driver for each port specified. All remaining drivers are tri-stated. When a port is write-enabled, it is actively driving the last value written to the port. If no values have been written to the port, all bits on the port will be actively driving a low.

CAUTION:

Damage to the Digital I/O card or the user's equipment could occur if the user write-enables the output driver for a port that is connected to a device that is also attempting to drive the data lines.

A port may be read while it is write-enabled and will return the current value that the port is driving. A port may be written to when tri-stated, but the value will not become present on the port until after it is write-enabled. It is the user's responsibility to correctly tri-state or write-enable the appropriate ports prior to synchronous operations.

Example:

The command:

SETUP 1.ENABLE,1,4-6,11

would cause ports 1, 4, 5, 6 and 11 to start actively driving values and would tri-state all the remaining ports.

SETUP RD command

Syntax: Byte: SE[TUP] <address>.RD,<port>[,Y][,B | ,H], <vectors>
Word: SE[TUP] <address>.RD,<port>,W[,B | ,H], <vectors>
Bit: SE[TUP] <address>.RD,<port>,X<bit> [,X<bit>...],<vectors>

<address>::= Module address of the 1260-14 (1-12)

<port>::= Synchronous port number that is being defined (0-11)

<vectors>::= The number of synchronous reads to perform (0-256)

<bit>::= Bit number to be read in the bit mode (0-7)

Description: This command sets up a synchronous port to perform a buffered read operation and clears that port's buffer of any previous values. Once a synchronous test is armed, data is clocked into the port by each active edge of CLKIN and the results stored in a buffer for up to a maximum of 256 vectors. A vector count of 0 implies that the port is to do nothing during this test. Once a test has been defined for a synchronous port, the test may be started and stopped at any time using the SETUP ARM ON/OFF commands. It should be noted that it is the user's responsibility to ensure that the appropriate ports are tri-stated before starting the synchronous test.

After the final data transfer has occurred for all synchronous ports, the ARM is automatically disabled, allowing the user to retrieve the buffered data via the PDATAOUT command. This is also allowed after a synchronous test is disarmed manually via the SETUP ARM OFF command.

Example 1:

Assume that ports 0 and 1 are defined as synchronous and the user sends the following commands:

```
SETUP 1.RD 0,Y,H,10

SETUP 1.RD 1,22
```

During the next synchronous test, port 0 would read 10 vectors worth of byte-wide information and store it in hexadecimal format. Port 1 would read 22 vectors of byte-wide information and store it in decimal format.

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Read operations may be performed as either bit, byte or word width operations, with byte width being the default. Data will be formatted in either decimal, hexadecimal or binary, with the default being decimal. The width and format of the output are specified as follows:

A "B" specifies that the output format for the data is binary.

An "H" specifies that the output format for the data is hexadecimal.

A "Y" specifies a byte-wide (8-bit) read of the port. If the port was previously read using a word width, the data associated with the companion port is cleared, and the port will be disabled in future synchronous operations until redefined. This is the default if no width is specified. See Example 1 above for a sample of a byte-wide synchronous read setup.

A "W" specifies a word-wide (16 bits) read of a pair of ports. Word-wide operations are specified on even-numbered ports only, and read the least significant 8 bits from the even port and the most significant 8 bits from the following odd-numbered port. Word-sized operations may not be mixed with bit or byte operations in either the even or odd port. If either the even or the odd port is redefined as a byte-wide or a bit-wide port, the matching odd or even companion port is disabled and should be redefined before the next test.

Example 2:

Assume that ports 0-3 are synchronous ports, ports 2 and 3 were previously defined as synchronous word-wide read ports and the user sends the following commands:

```
SETUP 1.RD 0,W,5

SETUP 1.RD 2,Y,7
```

The first command would cause the module to perform a word-wide read of five vectors worth of data from ports 0 and 1 during the next synchronous test. The second command would cause a byte-wide read of 7 vectors worth of data from port 2 during the next synchronous test, and would disable port 3 from participating in subsequent tests until redefined.

An "X" specifies a bit-wide read of the port. Any combination of the 8 bits from X0-X7 may be specified, but only the selected bits are stored when the user runs the synchronous test. The buffer will contain the status of the bits requested at each vector in the same order as specified in the command. If the port was previously read using a word width, the data associated with the companion port will be cleared, and the port will be disabled in future synchronous operations until redefined.

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Example 3:

Assume that port 0 is a synchronous port and the user sends the following command:

SETUP 1.RD 0,X5,X7,X1,10

This command would cause the module to perform a bit-wide read of bits 5, 7 and 1 for ten vector on port 0 during the next synchronous test.

SETUP SYNC command

Syntax: SE[TUP] <address> .SY[NC],<number of ports>

<address>::= Module address of the 1260-14 (1-12)

<number of ports>::= Number of ports to make synchronous (0-12)

Description: This command specifies the number of ports that will have the synchronous mode enabled. Note that the user may not specify which ports are synchronous and which are asynchronous. Instead, the synchronous ports are always grouped together starting at port 0; i.e., the first synchronous port is always port 0; the second is always port 1, etc.

Example:

Assume the user sends the following command:

SETUP 1.SYNC,5

This would cause the digital I/O card with the module address of 1 to define the 5 ports from port 0 to port 4 as synchronous ports. The remaining 7 ports from port 5 to port 11 would become asynchronous.

On power-up, the synchronous mode is disabled for all ports. When the SYNC command is given, those ports that change configuration from asynchronous to synchronous, or vice versa, are re-initialized. This causes any old format, mode, or read/write data to be removed. Consequently, all new synchronous ports should be programmed with a SETUP <address>.RD or SETUP <address>.WR command before they are used in synchronous operations.

Only those ports defined as synchronous may perform data transfers utilizing the CLKIN and BUSY handshake lines.

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The asynchronous WRITE command will work normally on a synchronous port, but the READ command will not. This allows the user to preset the value of the port prior to the beginning synchronous operations. Note that this may only be done while the synchronous mode is not armed.

SETUP WR command

Syntax:
Byte: SE[TUP] <address>.WR,<port>[,Y][,<byte>,...,<byte>]
Word: SE[TUP] <address>.WR,<port>[,W][,<word>,...,<word>]
Bit: SE[TUP] <address>.WR,<port>[,X][,<bits>;...;<bits>]

<address>::= Module address of the 1260-14 (1-12)

<port>::= Synchronous port number that is being defined (0-11)

<byte>::= An 8-bit value specified as either decimal format (0-255), hexadecimal format (H0-HFF) or binary format (B0-B11111111). Note that the "H" is required in front of hex values and the "B" is required in front of binary values.

<word>::= A 16-bit value specified in either decimal format (0-65535), hexadecimal format (H0-HFFFF) or binary format (B0-B1111111111111111). Note that the "H" is required in front of hex values and the "B" is required in front of binary values.

<bits>::= Specifies up to eight single bit transitions in the form Lx|Hx,...Lx|Hx where x specifies which bit number to write high (Hx) or low (Lx), and x may take the values from 0-7. For example, SETUP 5.WR 1,X,L1,L3;H0,H1 would cause bits 1 and 3 in port 1 to go low in vector 1 followed by bits 0 and 1 going high in vector 2.

Description: This command sets up a single synchronous port to perform a buffered write operation. Up to 256 data vectors can be set up ahead of time in the port's buffer. Once a synchronous test is armed, data from the buffer is clocked out of the port by each active edge of CLKIN until either the last data item for each synchronous port has been clocked, automatically disarming the test, or the user disarms the test manually using the SETUP ARM,OFF command. The last value on the port will remain there until either another synchronous test is run, the user performs an asynchronous WRITE on the port or the user resets the module. It should be noted that it is the user's responsibility to ensure that the appropriate ports are write-enabled before starting the synchronous test.

Write commands may be specified as either bit, byte or word-wide

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operations. When a width change is requested by using either the "W", "X" or "Y" width designator, the port's buffer is cleared of all previous data and the new data is loaded starting at vector 1. If there is no width designator, the port remains in its current mode, and the new data is appended to the existing data in the buffer for up to a maximum of 256 vectors of data. This means that multiple statements may be used to load a given port's buffer by specifying a width for the first SETUP WR statement, and not specifying a width for subsequent statements.

Example 1:

Assume the user sends the following three statements to the module:

```
SETUP 1.WR 0,Y,7,15,23
SETUP 1.WR 0,255
SETUP 1.WR 0,100
```

The first SETUP statement would set up port 0 to perform byte-wide operations and would clear the port 0 buffer of any previous values. It would then load a 7 in vector 1, a 15 in vector 2 and a 23 in vector 3. The second SETUP statement would leave the buffer intact, and would load a 255 in vector 4. The final SETUP statement would load a 100 in vector 5. Once the test was armed, port 0 would be actively driving a 7 after the first clock, a 15 after the second, etc. and would end the test driving a 100.

The data that is loaded in the buffer remains there until either the port is re-initialized by a SETUP WR or a WRITE command, the port is redefined to be a read port, the port is redefined to be an asynchronous port, or the unit is reset. This means that it is possible to arm and run a test multiple times without having to reload the write data.

Bit, byte and word-wide operations cannot be mixed in a port. Only one width may be active at a time and is specified as follows:

A "Y" specifies a byte-wide (8-bit) write to a port. If the port was previously defined using a word width, the data associated with the companion port will be cleared, and the port will be disabled in future synchronous operations until redefined. When a port is first defined as synchronous, it defaults to byte-wide operations, so it is only necessary to specify a byte width if the user is changing from a different width, or wishes to clear the buffer. See Example 1 above for a sample of a byte-wide synchronous write setup.

A "W" specifies a word-wide (16-bit) write to a pair of ports. Word-

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wide operations are specified on even-numbered ports only, and place the least significant 8 bits in the even port and the most significant 8 bits in the following odd-numbered port. Word sized operations may not be mixed with bit or byte operations in either the even or odd port. If either the even or the odd port is redefined as a byte-wide or a bit-wide port, both ports will have their buffers cleared and the matching odd or even companion port will be disabled in future synchronous operations until redefined.

Example 2:

Assume that ports 0-3 are synchronous ports, ports 2 and 3 were previously defined as synchronous word-wide write ports, and the user sends the following commands:

```
SETUP 1.WR 0,W,H5F01,H6F02,H7F03
SETUP 1.WR 2,Y,16,8,4,2,1
```

The first command would clear the buffers for ports 0 and 1, and would cause the module to perform a word-wide write of three vectors to ports 0 and 1 during the next synchronous test, finishing the test with the value of hex 03 in port 0 and hex 7F in port 1. The second command would clear the buffers for ports 2 and 3 and would cause a byte-wide write of five vectors to port 2 during the next synchronous test, finishing the test with a value of 1 in port 2. Port 3 would be disabled from participating in subsequent tests until redefined.

An "X" specifies a bit-wide write to a port. Any of the 8 bits from 0-7 may be set to 0 (Low) or 1 (High) by using the form Lx or Hx, where x is the bit to modify. Multiple bits may be modified by separating the bit transitions with commas. Multiple vectors may be set up by separating the changes for each vector with semicolons. Bits that are not modified remain in their previous states. If the port was previously defined using a word width, the data associated with the companion port will be cleared, and the port will be disabled in future synchronous operations until redefined.

Example 3:

Assume the user sends the following two statements to the module and the current value of port 0 is a binary 00000000:

```
SETUP 1.WR 0,X,H3;H1,L3;H5,H7
SETUP 1.WR 0,L1,L7
```

The first SETUP statement will first clear the buffer for port 0, then

specify that bit 3 will go high in vector 1, bit 1 will go high and bit 3 will go low in vector 2, and bits 5 and 7 will go high in vector 3. The second SETUP statement will leave the buffer intact and will specify that in vector 4, bits 1 and 7 will go low. Once the test is armed, port 0 would be actively driving a binary 00001000 after the first clock, a 00000010 after the second, a 10100010 after the third and a 00100000 after the last clock.

WRITE command

Syntax: Byte: WR[ITE] <address>.<ports>[,Y][,<byte>,..., <byte>]

Word: WR[ITE] <address>.<ports>[,W][,<word>,..., <word>]

Bit: WR[ITE] <address>.<ports>[,X][,<bits>;.....;<bits>]

<address>::= Module address of the 1260-14 (1-12)

<ports>::= One or more consecutive ports to write to. A single port is specified as a decimal number from 0 to 11. A group of ports is specified as two decimal numbers from 0 to 11 separated by a hyphen, (-), with the least significant port to the right and the most significant port to the left. For example, the command WR 1.3-5,Y,0,1,2 would write a 0 in port 3, a one in port 4 and a 2 in port 5. Data may be specified in decimal, hexadecimal or binary.

<byte>::= An 8-bit value specified as either decimal format (0-255), hexadecimal format (H0-HFF) or binary format (B0-B11111111). Note that the "H" is required in front of hex values and the "B" is required in front of binary values.

<word>::= A 16-bit value specified in either decimal format (0-65535), hexadecimal format (H0-HFFFF) or binary format (B0-B1111111111111111). Note that the "H" is required in front of hex values and the "B" is required in front of binary values.

<bits>::= Specifies up to eight single bit transitions in the form Lx|Hx,...Lx|Hx where x specifies which bit number to write high (Hx) or low (Lx), and x may take the values from 0-7. For example, WR 1.1-2,X,L1,L3;H0,H1 would cause bits 1 and 3 to go low in port 1 and bits 0 and 1 to go high in port 2.

Description: This command performs an asynchronous write to a single port or a group of consecutive ports. No handshaking is required for this operation. The command is primarily used to write to asynchronous ports, but may be used to preset synchronous ports to a known value before starting synchronous operations.

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NOTE:

Care should be used not to change the width when writing to a synchronous port if the port has already had its width defined and data loaded into the buffer. In this case, the user should not specify a width, and should format the WRITE data in the same size that the synchronous port was defined at. Failure to do so will cause the port to change its width designation, and will clear the data in the buffer.

As soon as the command is received, an immediate write to the specified ports occurs. A port may be written to when tri-stated, but the value will not become present on the port until after it is write-enabled. The data is written one data item per port, and the number of ports must match the number of data items. The first data item corresponds to the lowest significant port and the last data item corresponds to the highest significant port.

Example 1:

Assume that ports 5-11 are defined as asynchronous and the user sends the following command:

WR 1.5-7,Y,23,0,127

At the end of command execution, port 5 would be actively driving a 23, port 6 would be driving 0 and port 7 would be driving 127.

Write operations may be performed as either a bit, byte or word-wide operation. If no width is specified, it remains unchanged from its previous setting, and the data must be specified in the same form as used in the most recent WRITE or SETUP WR statement for each port. If no width has ever been specified, the default is byte-wide. Bit, byte and word-wide operations cannot be mixed in a port. Only one width is active at a time and is specified as follows:

A "Y" causes a byte-wide (8-bit) write to the ports. When writing to a synchronous port that was previously defined or written to using a word width, the data buffer associated with the companion port will be cleared and the port will be disabled in future synchronous operations until it is redefined. When a port is first defined as synchronous or asynchronous, it defaults to byte-wide operations, so it is only necessary to specify the byte width if the user is changing from a different width, or wishes to clear the synchronous write buffer. See Example 1 above for a sample of a byte-wide asynchronous write.

A "W" causes a word-wide (16-bit) write to pairs of ports. Word-

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wide operations are specified on even-numbered ports only, and place the least significant 8 bits in the even-numbered port and the most significant 8 bits in the following odd-numbered port. Word-wide operations may not be mixed with bit or byte-wide operations in either the even or odd port.

Example 2:

Assume that ports 5-11 are defined as asynchronous and the user sends the following command:

```
WR 1.8,W,H23A7
```

At the end of command execution, port 8 would be actively driving a hex 23 and port 9 would be driving hex A7.

An "X" specifies a bit-wide write to the ports. Any of the 8 bits within a port may be set to 0 (Low) or 1 (High) by using the form Lx or Hx, where x is the bit (0-7) to modify within the byte. Multiple bits within a port may be modified by separating the bit transitions with commas. Multiple ports may be modified by separating the changes for each port with semicolons. Bits that are not modified, remain in their previous states. When writing to a synchronous port that was previously defined or written to using a word width, the data buffer associated with the companion port will be cleared and the port will be disabled in future synchronous operations until it is redefined.

Example 3:

Assume that all ports are asynchronous, the current value of port 0 and port 1 is a binary 00000000, and the user sends the following statements to the module:

```
WR 1.0-1,X,H3;H1,H7
WR 1.0-1,L3,H5;L1,H6
```

After the execution of the first command, port 0 would be actively driving a binary 00001000 and port 1 would be driving a 10000010. After the second command, port 0 would be driving a 00100000 and port 2 would be driving a 11000000. Note that in the second command, there was no width specified since it was not required.

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Synchronous Mode Example

The following is an example of an 8-vector synchronous read/write operation using a 1260-14 at address 1:

1. SE 1.SY,2<CR><LF>	Sets up ports 0 and 1 for SYNC mode; ports 2-11 will be in ASYNC mode.
2. SE 1.RD 0,8<CR><LF>	Tells the module to read data into first eight buffer locations of port 0 when clocked.
3. SE 1.WR 1,Y,1,2,3,4<CR><LF>	Sets port 1 into the byte mode and loads write data into its first four buffer locations.
4. SE 1.WR 1,5,6,7,8<CR><LF>	Loads write data into the next four buffer locations of port 1.
5. WR 1.1,0<CR><LF>	Presets the value of port 1 to zero.
6. SE 1.EN,1<CR><LF>	Write enables port 1.

Now the 1260-14 has write data in the first eight buffer locations for port 1.

7. SE 1.AR, ON<CR><LF>	Enable SYNC handshake of READ/WRITE.

Eight handshakes occur using the CLKIN and BUSY lines, with each one causing a READ/WRITE to/from ports 0/1 for the eight programmed buffer locations. The eighth clock input causes the 1260-14 to disarm and stops all handshaking until the unit is rearmed.

8. PD 1.0<CR><LF>	Reads the data from the 1260-14.

Repeat Steps 3-8 to reprogram and run using a new set of WRITE data, or repeat Steps 5, 7 and 8 to re-execute the same test.

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Chapter 4

OPTIONAL HARNESS ASSEMBLIES

The following harness assemblies are used to connect 1260-14 to Freedom Series Test Receiver Interfaces.

Each harness documentation consists of an assembly drawing, parts list, system wire list and wire list.

407272 Virginia Panel, Inc. Series VP90 Interface Harness

407273 TTI Testron, Inc. Interface Harness

For more information on complete line of Test Receivers Interface solution, contact your Sales Representative.

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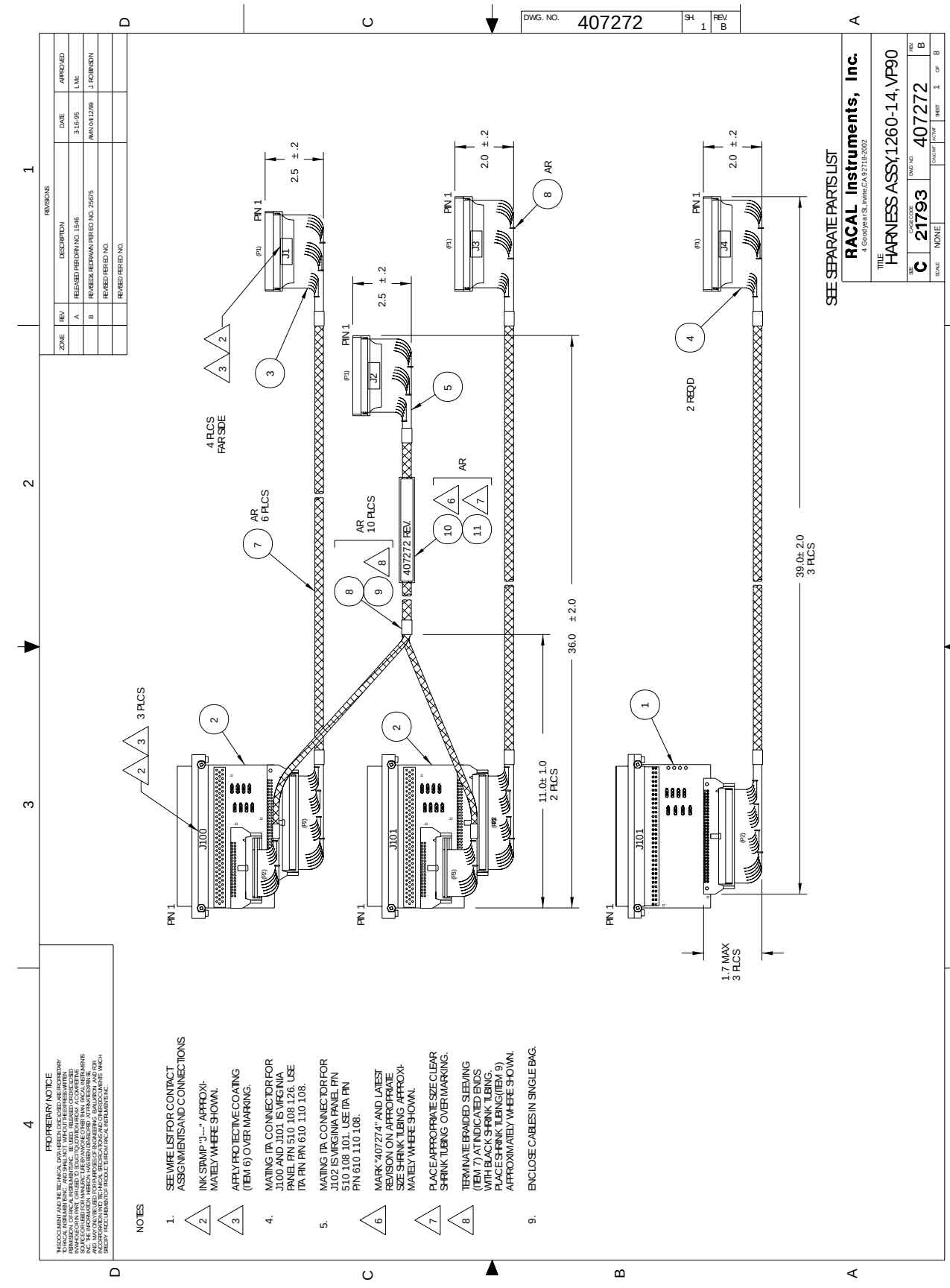
DWG. NO. 407272
SH. 1
REV. B
SEE SEPARATE PARTS LIST
RACAL Instruments, Inc.
4 Goodyear St., Irvine, CA 92718-2002
TITLE
HARNESS ASSY,1260-14,VP90
SIZE C
CAGE CODE 21793
DWG NO. 407272
REV B
SCALE NONE
SHEET 1 OF 8
98 0337 REV. F
REVISIONS
ZONE
REV
DESCRIPTION
DATE
APPROVED
A
RELEASED PER DRN NO. 1546
3-16-95
L Mc
B
REVISED& REDRAWN PER EO NO. 25675
AMN 04/12/99
J. ROBINSON
REVISED PER EO NO.
REVISED PER EO NO.
PROPRIETARY NOTICE
NOTES
1. SEE WIRE LIST FOR CONTACT ASSIGNMENTS AND CONNECTIONS
2 INK STAMP "J---" APPROXIMATELY WHERE SHOWN.
3 APPLY PROTECTIVE COATING (ITEM 6) OVER MARKING.
4. MATING ITA CONNECTOR FOR J100 AND J101 IS VIRGINIA PANEL P/N 510 108 126. USE ITA P/N P/N 610 110 108.
5. MATING ITA CONNECTOR FOR J102 IS VIRGINIA PANEL P/N 510 108 101. USE ITA P/N P/N 610 110 108.
6 MARK "407274" AND LATEST REVISION ON APPROPRIATE SIZE SHRINK TUBING APPROXIMATELY WHERE SHOWN.
7 PLACE APPROPRIATE SIZE CLEAR SHRINK TUBING OVER MARKING.
8 TERMINATE BRAIDED SLEEVING (ITEM 7) AT INDICATED ENDS WITH BLACK SHRINK TUBING. PLACE SHRINK TUBING(ITEM 9) APPROXIMATELY WHERE SHOWN.
9. ENCLOSE CABLES IN SINGLE BAG.
J100
J101
J1
J2
J3
J4
PIN 1
2.5 ± .2
2.0 ± .2
4 PLCS FAR SIDE
AR 6 PLCS
AR 10 PLCS
AR
407272 REV.
2 REQ'D
3 PLCS
36.0 ± 2.0
11.0± 1.0 2 PLCS
39.0± 2.0 3 PLCS
1.7 MAX 3 PLCS

ENGINEERING PARTS LIST

ITEM	BIN	PART NO.	DESCRIPTION	U/M	QTY	REFERENCE
1		405084	PCB AS SY, VP90 INTFC,64PIN	EA	1.00000	J102
2		405085	PCB ASSY, VP90 1NTFC,96PIN	EA	2.00000	J100-J101
3		407251	CABLE ASSY, DC, 50-COND., VP90	EA	1.00000	
4		407256	CABLE ASSY, DC, 60-COND., VP90	EA	2.00000	
5		407252	CABLE ASS Y, 50SPLT, VP90	EA	1.00000	
6		910541	POLYURETHANE CONF. COAT	EA	.00001	
7		GRP-110-1/2	TBGOV-Poy.250ID-BLACK	FT	.00001	
8		500005	TIE CORD NYLON	FT	.00001	
9		500017	TBGSRK-POF.500ID-BLACK	FT	.00001	
10		M23053/5-109-4	TBGSRK-POF.750ID-YELLOW	FT	.00001	
11		500104	TBGSRK-POF.750ID-CLEAR	FT	.00001	

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ENGINEERING PARTS LIST

WIRE	FROM	TO	TYPE	PART #	WIRE LEN	REFERENCE
	BLK AA (J100)	Uxx-SLOT yy (J1,J2)	CABLE	407272		SYSTEM WIRE LIST
	BLK AA (J101)	Uxx-SLOT yy (J2,J3)	CABLE	407272		
	BLK AA (J102)	Uxx-SLOT yy (J4)	CABLE	407272		

This system wirelist serves as a template for incorporating this harness assembly into the overall system wirelist. It does not in any way affect the fabrication of this harness assembly.

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DOCUMENT TITLE	SIZE.	CODE NO	DOCUMENT NO.	REV
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	DRN			SHEET 3 of 9

ENGINEERING WIRE LIST

WIRE	FROM	TO	TYPE	PART #	WIRE LEN	REFERENCE
1	J100-96	J1-1	BRN	407251	41.5"	CHAN 01
2	J100-32	J1-2	TAN	407251	41.5"	CHAN 01 RTN
3	J100-64	J1-3	RED	407251	41.5"	CHAN 02
4	J100-95	J1-4	TAN	407251	41.5"	CHAN 02 RTN
5	J100-31	J1-5	ORN	407251	41.5"	CHAN 03
6	J100-63	J1-6	TAN	407251	41.5"	CHAN 03 RTN
7	J100-94	J1-7	YEL	407251	41.5"	CHAN 04
8	J100-30	J1-8	TAN	407251	41.5"	CHAN 04 RTN
9	J100-62	J1-9	ORN	407251	41.5"	CHAN 05
10	J100-93	J1-10	TAN	407251	41.5"	CHAN 05 RTN
11	J100-29	J1-11	BLU	407251	41.5"	CHAN 06
12	J100-61	J1-12	TAN	407251	41.5"	CHAN 06 RTN
13	J100-92	J1-13	VIO	407251	41.5"	CHAN 07
14	J100-28	J1-14	TAN	407251	41.5"	CHAN 07 RTN
15	J100-60	J1-15	GRY	407251	41.5"	CHAN 08
16	J100-91	J1-16	TAN	407251	41.5"	CHAN 08 RTN
17	J100-27	J1-17	WRT	407251	41.5"	CHAN 09
18	J100-59	J1-18	TAN	407251	41.5"	CHAN 09 RTN
19	J100-90	J1-19	BLK	407251	41.5"	CHAN 10
20	J100-26	J1-20	TAN	407251	41.5"	CHAN 10 RTN
21	J100-58	J1-21	BRN	407251	41.5"	CHAN 11
22	J100-89	J1-22	TAN	407251	41.5"	CHAN 11 RTN
23	J100-25	J1-23	RED	407251	41.5"	CHAN 12
24	J100-57	J1-24	TAN	407251	41.5"	CHAN 12 RTN
25	J100-88	J1-25	ORN	407251	41.5"	CHAN 13
26	J100-24	J1-26	TAN	407251	41.5"	CHAN 13 RTN
27	J100-56	J1-27	YEL	407251	41.5"	CHAN 14
28	J100-87	J1-28	TAN	407251	41.5"	CHAN 14 RTN
29	J100-23	J1-29	GRN	407251	41.5"	CHAN 15
30	J100-55	J1-30	TAN	407251	41.5"	CHAN 15 RTN
31	J100-86	J1-31	BLU	407251	41.5"	CHAN 16
32	J100-22	J1-32	TAN	407251	41.5"	CRAN 16 RTN
33	J100-54	J1-33	VIO	407251	41.5"	CHAN 17
34	J100-85	J1-34	TAN	407251	41.5"	CHAN 17 RTN
35	J100-21	J1-35	GRY	407251	41.5"	CHAN 18
36	J100-53	J1-36	TAN	407251	41.5"	CHAN 18 RTN
37	J100-84	J1-37	WHT	407251	41.5"	CHAN 19
38	J100-20	J1-38	TAN	407251	41.5"	CHAN 19 RTN
39	J100-52	J1-39	BLK	407251	41.5"	CHAN 20
40	J100-83	J1-40	TAN	407251	41.5"	CHAN 20 RTN
41	J100-19	J1-41	BRN	407251	41.5"	CHAN 21
42	J100-51	J1-42	TAN	407251	41.5"	CHAN 21 RTN
43	J100-82	J1-43	RED	407251	41.5"	CHAN 22
44	J100-18	J1-44	TAN	407251	41.5"	CHAN 22 RTN
45	J100-50	J1-45	ORN	407251	41.5"	CHAN 23
46	J100-81	J1-46	TAN	407251	41.5"	CHAN 23 RTN
47	J100-17	J1-47	YEL	407251	41.5"	CHAN 24
48	J100-49	J1-48	TAN	407251	41.5"	CHAN 24 RTN
49	J100-80	J1-49	GRN	407251	41.5"	BUSY
50	J100-16	J1-50	TAN	407251	41.5"	GND

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ENGINEERING WIRE LIST

WIRE	FROM	TO	TYPE	PART #	WIRE LEN	REFERENCE
51 52	J100-48 J100-79	NO CONNECT NO CONNECT				
53 54	J100-15 J100-47	NO CONNECT NO CONNECT				
55 56	J100-78 J100-14	NO CONNECT NOCONNECT				
57 58	J100-46 J100-77	NO CONNECT NO CONNECT				
59 60	J100-13 J100-45	NO CONNECT NO CONNECT				
61 62	J100-76 J100-12	NO CONNECT NO CONNECT				
63 64	J100-44 J100-75	NO CONNECT NO CONNECT				
65 66	J100-11 J100-43	NO CONNECT NO CONNECT				
67 68	J100-74 J100-10	NO CONNECT NO CONNECT				
69 70	J100-42 J100-73	NO CONNECT NO CONNECT				
71 72	J100-9 J100-41	J2-1 J2-2	BRN TAN	407252 407252	41.5" 41.5"	CHAN 25 CHAN 25 RTN
73 74	J100-72 J100-8	J2-3 J2-4	RED TAN	407252 407252	41.5" 41.5"	CHAN 26 CHAN 26 RTN
75 76	J100-40 J100-71	J2-5 J2-6	ORN TAN	407252 407252	41.5" 41.5"	CHAN 27 CHAN 27 RTN
77 78	J100-7 J100-39	J2-7 J2-8	YEL TAN	407252 407252	41.5" 41.5"	CHAN 28 CHAN 28 RTN
79 80	J100-70 J100-6	J2-9 J2-10	GRN TAN	407252 407252	41.5" 41.5"	CHAN 29 CHAN 29 RTN
81 82	J100-38 J100-69	J2-11 J2-12	BLU TAN	407252 407252	41.5" 41.5"	CHAN 30 CHAN 30 RTN
83 84	J100-5 J100-37	J2-13 J2-14	VIO TAN	407252 407252	41.5" 41.5"	CHAN 31 CHAN 31 RTN
85 86	J100-68 J100-4	J2-15 J2-16	GRY TAN	407252 407252	41.5" 41.5"	CHAN 32 CHAN 32 RTN
87 88	J100-36 J100-67	J2-17 J2-18	WHT TAN	407252 407252	41.5" 41.5"	CHAN 33 CHAN 33 RTN
89 90	J100-3 J100-35	J2-19 J2-20	BLK TAN	407252 407252	41.5" 41.5"	CHAN 34 CHAN 34 RTN
91 92	J100-66 J100-2	J2-21 J2-22	BRN TAN	407252 407252	41.5" 41.5"	CHAN 35 CHAN 35 RTN
93 94	J100-34 J100-65	J2-23 J2-24	RED TAN	407252 407252	41.5" 41.5"	CHAN 36 CHAN 36 RTN
95 96	J100-1 J100-33	J2-25 J2-26	ORN TAN	407252 407252	41.5" 41.5"	CHAN 37 CHAN 37 RTN

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ENGINEERING WIRE LIST

WIRE	FROM	TO	TYPE	PART #	WIRE LEN	REFERENCE
97 98	J101-72 J101-8	J2-27 J2-28	YEL TAN	407252 407252	41.5" 41.5"	CHAN 38 CHAN 38 RTN
99 100	J10140 J101-71	J2-29 J2-30	GRN TAN	407252 407252	41.5" 41.5"	CHAN 39 CHAN 39 RTN
101 102	J101-7 J101-39	J2-31 J2-32	BLU TAN	407252 407252	41.5" 41.5"	CHAN 40 CHAN 40 RTN
103 104	J101-70 J101-6	J2-33 J2-34	VIO TAN	407252 407252	41.5" 41.5"	CHAN 41 CHAN 41 RTN
105 106	J101-38 J101-69	J2-35 J2-36	GRY TAN	407252 407252	41.5" 41.5"	CHAN 42 CHAN 42 RTN
107 108	J101-5 J101-37	J2-37 J2-38	WHT TAN	407252 407252	41.5" 41.5"	CHAN 43 CHAN 43 RTN
109 110	J101-68 J101-4	J2-39 J2-40	BLK TAN	407252 407252	41.5" 41.5"	CHAN 44 CHAN 44 RTN
111 112	J101-36 J101-67	J2-41 J2-42	BRN TAN	407252 407252	41.5" 41.5"	CHAN 45 CHAN 45 RTN
113 114	J101-3 J101-35	J2-43 J2-44	RED TAN	407252 407252	41.5" 41.5"	CHAN 46 CHAN 46 RTN
115 116	J101-66 J101-2	J245 J2-46	ORN TAN	407252 407252	41.5" 41.5"	CHAN 47 CHAN 47 RTN
117 118	J101-34 J101-65	J2-47 J2-48	YEL TAN	407252 407252	41.5" 41.5"	CHAN 48 CHAN 48 RTN
119 120	J101-1 J101-3;	J2-49 J2-50	GRN TAN	407252 407252	41.5" 41.5"	CLOCK IN CLOCK IN RTN
121 122	J101-96 J101-32	J3-1 J3-2	BRN TAN	407256 407256	41.5" 41.5"	CHAN 49 CHAN 49 RTN
123 124	J101-64 J101-95	J3-3 J3-4	RED TAN	407256 407256	41.5" 41.5"	CHAN 50 CHAN 50 RTN
125 126	J101-31 J101-63	J3-5 J3-6	ORN TAN	407256 407256	41.5" 41.5"	CHAN 51 CHAN 51 RTN
127 128	J101-94 J101-30	J3-7 J3-8	YEL TAN	407256 407256	41.5" 41.5"	CHAN 52 CHAN 52 RTN
129 130	J101-62 J101-93	J3-9 J3-10	GRN TAN	407256 407256	41.5" 41.5"	CHAN 53 CHAN 53 RTN
131 132	J101-29 J101-61	J3-11 J3-12	BLU TAN	407256 407256	41.5" 41.5"	CHAN 54 CHAN 54 RTN
133 134	J101-92 J101-28	J3-13 J3-14	VIO TAN	407256 407256	41.5" 41.5"	CHAN 55 CHAN 55 RTN
135 136	J101-60 J101-91	J3-15 J3-16	GRY TAN	407256 407256	41.5" 41.5"	CHAN 56 CHAN 56 RTN
137 138	J101-27 J101-59	J3-17 J3-18	WHT TAN	407256 407256	41.5" 41.5"	CHAN 57 CHAN 57 RTN
139 140	J101-90 J101-26	J3-19 J3-20	BLK TAN	407256 407256	41.5" 41.5"	CHAN 58 CHAN 58 RTN
141 142	J101-58 J101-89	J3-21 J3-22	BRN TAN	407256 407256	41.5" 41.5"	CHAN 59 CHAN 59 RTN
143 144	J101-25 J101-57	J3-23 J3-24	RED TAN	407256 407256	41.5" 41.5"	CHAN 60 CHAN 60 RTN

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ENGINEERING WIRE LIST

WIRE	FROM	TO	TYPE	PART #	WIRE LEN	REFERENCE
145 146	J101-88 J101-24	J3-25 J3-26	ORN TAN	407256 407256	41.5" 41.5"	CHAN 61 CHAN 61 RTN
147 148	J101-56 J101-87	J3-27 J3-28	YEL TAN	407256 407256	41.5" 41.5"	CHAN 62 CHAN 62 RTN
149 150	J101-23 J101-55	J3-29 J3-30	ORN TAN	407256 407256	41.5" 41.5"	CHAN 63 CHAN 63 RTN
151 152	J101-86 J101-22	J3-31 J3-32	BLU TAN	407256 407256	41.5" 41.5"	CHAN 64 CHAN 64 RTN
153 154	J101-54 J101-85	J3-33 J3-34	VIO TAN	407256 407256	41.5" 41.5"	CHAN 65 CHAN 65 RTN
155 156	J101-21 J101-53	J3-35 J3-36	GRY TAN	407256 407256	41.5" 41.5"	CHAN 66 CHAN 66 RTN
157 158	J101-84 J101-20	J3-37 J3-38	WHT TAN	407256 407256	41.5" 41.5"	CHAN 67 CHAN 67 RTN
159 160	J101-52 J101-83	J3-39 J3-40	BLK TAN	407256 407256	41.5" 41.5"	CHAN 68 CHAN 68 RTN
161 162	J101-19 J101-51	J3-41 J3-42	BRN TAN	407256 407256	41.5" 41.5"	CHAN 69 CHAN 69 RTN
163 164	J101-82 J101-18	J3-43 J3-44	RED TAN	407256 407256	41.5" 41.5"	CHAN 70 CHAN 70 RTN
165 166	J101-50 J101-81	J3-45 J3-46	ORN TAN	407256 407256	41.5" 41.5"	CIIAN 71 CHAN 71 RTN
167 168	J101-17 J101-49	J3-47 J3-48	YEL TAN	407256 407256	41.5" 41.5"	CHAN 72 CHAN 72 RTN
169 170	J101-80 J101-16	J3-49 J3-50	GRN TAN	407256 407256	41.5" 41.5"	EDRVR 00/VEXT 01 EDRVR 00/VEXT 01 RTN
171 172	J101-48 J101-79	J3-51 J3-52	BLU TAN	407256 407256	41.5" 41.5"	EDRVR 01/VEXT 02 EDRVR 01/VEXT 02 RTN
173 174	J101-15 J101-47	J3-53 J3-54	VIO TAN	407256 407256	41.5" 41.5"	EDRVR 02/VEXT 03 EDRVR 02/VEXT 03 RTN
175 176	J101-78 J101-14	J3-55 J3-56	GRY TAN	407256 407256	41.5" 41.5"	EDRVR 03/VEXT 04 EDRVR 03/VEXT 04 RTN
177 178	J101-46 J101-77	J3-57 J3-58	WHT TAN	407256 407256	41.5" 41.5"	EDRVR 04/VEKT 05 EDRVR 04/VEXT 05 RTN
179 180	J101-13 J101-45	J3-59 J3-60	BLK TAN	407256 407256	41.5" 41.5"	EDRVR 05/VEXT 06 EDRVR 05/VEXT 06 RTN
181 182	J101-76 J101-12	NO CONNECT NO CONNECT				
183 184	J101-44 J101-75	NO CONNECT NO CONNECT				
185 186	J101-11 J101-43	NO CONNECT NO CONNECT				
187 188	J101-74 J101-10	NO CONNECT NO CONNECT				
189 190	J101-42 J101-73	NO CONNECT NO CONNECT				
191 192	J101-9 J101-41	NO CONNECT NO CONNECT				

RACAL Instruments, Inc., 4 Goodyear St., Irvine, CA 92718

DOCUMENT TI'LE	SIZE.	CODE NO	DOCUMENT NO.	REV
HARNESS ASSY, 1260-14,VP90	A	21793	407272	B
	DRN			SHEET 7 of 9

ENGINEERING WIRE LIST

WIRE	FROM	TO	TYPE	PART #	WIRE LEN	REFERENCE
193	J102-64	J4-1	BRN	407256	41.5"	CHAN 73
194	J102-32	J4-2	TAN	407256	41.5"	CHAN 73 RTN
195	J102-63	J4-3	RED	407256	41.5"	CHAN 74
196	J102-31	J4-4	TAN	407256	41.5"	CHAN 74 RTN
197	J102-62	J4-5	ORN	407256	41.5"	CHAN 75
198	J102-30	J4-6	TAN	407256	41.5"	CHAN 75 RTN
199	J102-61	J4-7	YEL	407256	41.5"	CHAN 76
200	J102-29	J4-8	TAN	407256	41.5"	CHAN 76 RTN
201	J102-60	J4-9	GRN	407256	41.5"	CHAN 77
202	J102-28	J4-10	TAN	407256	41.5"	CHAN 77 RTN
203	J102-59	J4-11	BLU	407256	41.5"	CHAN 78
204	J102-27	J4-12	TAN	407256	41.5"	CHAN 78 RTN
205	J102-58	J4-13	VIO	407256	41.5"	CHAN 79
206	J102-26	J4-14	TAN	407256	41.5"	CHAN 79 RTN
207	J102-57	J4-15	GRY	407256	41.5"	CHAN 80
208	J102-25	J4-16	TAN	407256	41.5"	CHAN 80 RTN
209	J102-56	J4-17	WHT	407256	41.5"	CHAN 81
210	J102-24	J4-18	TAN	407256	41.5"	CHAN 81 RTN
211	J102-55	J4-19	BLK	407256	41.5"	CHAN 82
212	J102-23	J4-20	TAN	407256	41.5"	CHAN 82 RTN
213	J102-54	J4-21	BRN	407256	41.5"	CHAN 83
214	J102-22	J4-22	TAN	407256	41.5"	CHAN 83 RTN
215	J102-53	J4-23	RED	407256	41.5"	CHAN 84
216	J102-21	J4-24	TAN	407256	41.5"	CHAN 84 RTN
217	J102-52	J4-25	ORN	407256	41.5"	CHAN 85
218	J102-20	J4-26	TAN	407256	41.5"	CHAN 85 RTN
219	J102-51	J4-27	YEL	407256	41.5"	CHAN 86
220	J102-19	J4-28	TAN	407256	41.5"	CHAN 86 RTN
221	J102-50	J4-29	GRN	407256	41.5"	CHAN 87
222	J102-18	J4-30	TAN	407256	41.5"	CHAN 87 RTN
223	J102-49	J4-31	BLU	407256	41.5"	CHAN 88
224	J102-17	J4-32	TAN	407256	41.5"	CHAN 88 RTN
225	J102-48	J4-33	VIO	407256	41.5"	CHAN 89
226	J102-16	J4-34	TAN	407256	41.5"	CHAN 89 RTN
227	J102-47	J4-35	GRY	407256	41.5"	CHAN 90
228	J102-15	J4-36	TAN	407256	41.5"	CHAN 90 RTN
229	J102-46	J4-37	WHT	407256	41.5"	CHAN 91
230	J102-14	J4-38	TAN	407256	41.5"	CHAN 91 RTN
231	J102-45	J4-39	BLK	407256	41.5"	CHAN 92
232	J102-13	J440	TAN	407256	41.5"	CHAN 92 RTN
233	J102-44	J441	BRN	407256	41.5"	CHAN 93
234	J102-12	J442	TAN	407256	41.5"	CHAN 93 RTN
235	J102-43	J443	RED	407256	41.5"	CHAN 94
236	J102-11	J444	TAN	407256	41.5"	CHAN 94 RTN
237	J102-42	J4-45	ORN	407256	41.5"	CHAN 95
238	J102-10	J446	TAN	407256	41.5"	CHAN 95 RTN
239	J102-41	J447	YEL	407256	41.5"	CHAN 96
240	J102-9	J448	TAN	407256	41.5"	CHAN 96 RTN
241	J102-40	J449	GRN	407256	41.5"	EDRVR 06/VEXT 07
242	J102-8	J4-50	TAN	407256	41.5"	EDRVR 06/VEXT 07 RTN

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DOCUMENT TI'LE	SIZE.	CODE NO	DOCUMENT NO.	REV
HARNESS ASSY, 1260-14,VP90	A	21793	407272	B
	DRN			SHEET 8 of 9

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ENGINEERING WIRE LIST

WIRE	FROM	TO	TYPE	PART #	WIRE LEN	REFERENCE
243 244	J102-39 J102-7	J4-51 J4-52	BLU TAN	407256 407256	41.5" 41.5"	EDRVR 07IVEXT 08 EDRVR 07IVEXT 08 RTN
245 246	J102-38 J102-6	J4-53 J4-54	VIO TAN	407256 407256	41.5" 41.5"	EDRVR 08/VEXT 09 EDRVR 08/VEXT 09 RTN
247 248	J102-37 J102-5	J4-55 J4-56	GRY TAN	407256 407256	41.5" 41.5"	EDRVR 09/VEXT 10 EDRVR 09/VEXT 10 RTN
249 250	J102-36 J1024	J4-57 J4-58	WHT TAN	407256 407256	41.5" 41.5"	EDRVR 10/VEXT 11 EDRVR 10/VENT 11 RTN
251 252	J102-35 J102-3	J4-59 J4-60	BLK TAN	407256 407256	41.5" 41.5"	EDRVR 11/VEXT 12 EDRVR 11/VEXT 12 RTN
253 254	J102-34 J102-2	NO CONNECT NO CONNECT				
255 256	J102-33 J102-1	NO CONNECT NO CONNECT				

RACAL Instruments, Inc., 4 Goodyear St., Irvine, CA 92718				
DOCUMENT TITLE	SIZE.	CODE NO	DOCUMENT NO.	REV
HARNESS ASSY, 1260-14,VP90	A	21793	407272	B
	DRN		SHEET 9 of 9	

PROPRIETARY NOTICE

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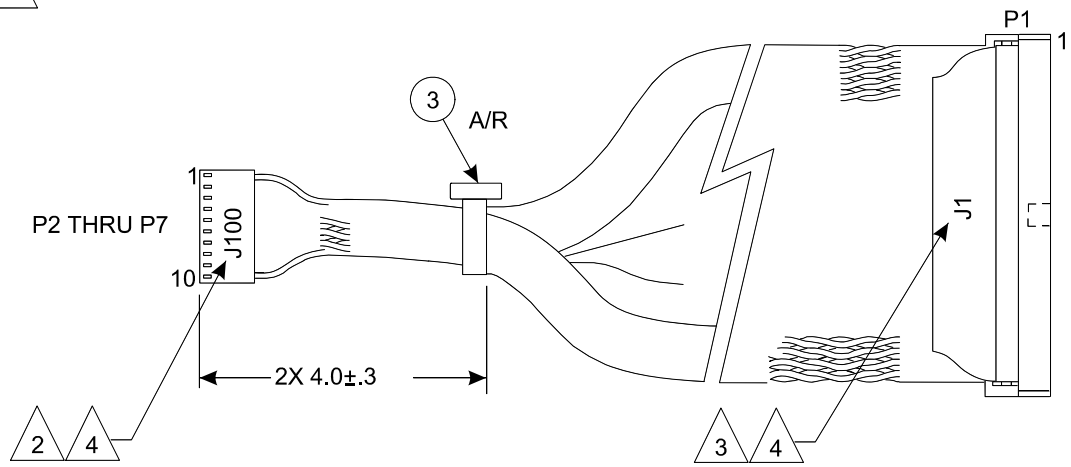
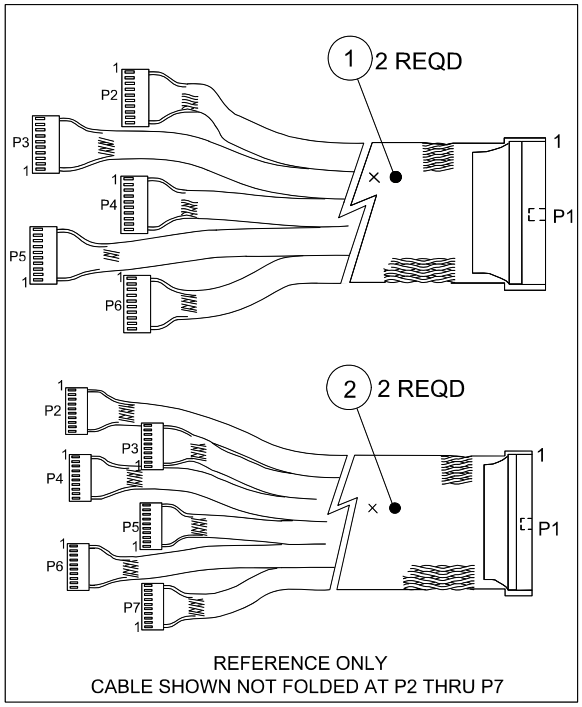
CONNECTOR MARKING TABULATION

CONNECTOR	CABLE #1 ①	CABLE #2 ①	CABLE #3 ②	CABLE #4 ②
(P1)	J1	J2	J3	J4
(P2)	J100	J105	J110	J116
(P3)	J101	J106	J111	J117
(P4)	J102	J107	J112	J118
(P5)	J103	J108	J113	J119
(P6)	J104	J109	J114	J120
(P7)			J115	J121

NOTES:

1. CONNECTOR P2 THRU P7 TO BE FOLDED SO THAT PIN #1 IS AT ONE SIDE OF CABLE ONLY.
2. WHITE INK STAMP J--- PER TABULATION AT P2 THRU P7 APPROXIMATELY WHERE SHOWN.
3. BLACK INK STAMP J- PER TABULATION AT P1 APPROXIMATELY WHERE SHOWN.
4. SPRAY PROTECTIVE COATING (ITEM 4) AFTER MARKING.
5. BUILD EACH CABLE ASSY SEPARATELY (4 TOTAL)
6. ENCLOSE CABLES IN SINGLE BAG AND IDENTIFY WITH PART NUMBER AND CURRENT REVISION.
7. CONNECTOR J100-121 WILL LATER CONNECT TO RECEIVER BLOCK, TTI P/N VGRCB-170H-R. MATING ITA CONNECTOR BLOCK IS TTI P.N VGFCB - 170.





RACAL Instruments, Inc.
4 Goodyear St., Irvine, Ca 92718-2002

TITLE
HARNESS ASSY, 1260-14,TTI

SIZE	CODE IDENT. NO.	DOCUMENT NO.	REV.
B	21793	407273	A

SCALE | SHEET 1 OF 8

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ENGINEERING PARTS LIST

ITEM	BIN	PART NO.	DESCRIPTION	QTY	REFERENCE
1		407250	CABLE ASSY, IDC, 50-COND, TTI	2	
2		407255	CABLE ASSY, IDC, 60-COND, TTI	2	
3		610777	TIE-CA-LKG-.062-.075	A/R	
4		910541	POLYURETHANE CONFORMAL COAT	A/R	

RACAL Instruments, Inc., 4 Goodyear St., Irvine, CA 92718				
DOCUMENT TI'LE	SIZE.	CODE NO	DOCUMENT NO.	REV
HARNESS ASSY, 1260-14,TTI	A	21793	407273	A
	DRN		SHEET 2 of 8	

ENGINEERING WIRE LIST

WIRE	FROM	TO	TYPE	PART #	WIRE LEN	REFERENCE
	BLK AAx RW 0l (J100)	Uxx-SLOT yy (JI)	CABLE	407273		SYSTEM WIRE LIST
	BLK AAx RW 02 (3101)	Uxx-SLOT yy (J1)	CABLE	407273		
	BLK AAx RW 03 (J102)	Uxx-SLOT yy (J1)	CABLE	407273		
	BLK AAx RW 04 (J103)	Uxx-SLOT yy (JI)	CABLE	407273		
	BLK AAx Rw 05 (J104)	Uxx-S LOT yy (J1)	CABLE	407273		
	BLK AAx RW 06 (J105)	Uxx-S LOT yy (J2)	CABLE	407273		
	BLK AAx RW 07 (J106)	Uxx-SLOT yy (J2)	CABLE	407273		
	BLK AAx RW 08 (J107)	Uxx-SLOT yy (J2)	CABLE	407273		
	BLK AAx RW 09 (J108)	Uxx-SLOT yy (J2)	CABLE	407273		
	BLK AAx RW 10 (J109)	Uxx-SLOT yy (J2)	CABLE	407273		
	BLK AAx RW 11 (J110)	Uxx-SLOT yy (J3)	CABLE	407273		
	BLK AAx RW 12 (J111)	Uxx-SLOT yy (J3)	CABLE	407273		
	BLK AAx RW 13 (J112)	Uxx-SLOT yy (J3)	CABLE	407273		
	BLK AAx RW 14 (J113)	Uxx-SLOT yy (J3)	CABLE	407273		
	BLK AAx RW 15 (J114)	Uxx-SLOT yy (J3)	CABLE	407273		
	BLK AAx RW 16 (J115)	Uxx-SLOT yy (J3)	CABLE	407273		
	BLK AAx RW 17 (J116)	Uxx-SLOT yy (J4)	CABLE	407273		
	BLK AAx RW 0l (J117)	Uxx-SLOT yy (J4)	CABLE	407273		
	BLK AAx RW 02 (J118)	Uxx-SLOT yy (J4)	CABLE	407273		
	BLK AAx RW 03 (J119)	Uxx-SLOT yy (J4)	CABLE	407273		
	BLK AAx RW 04 (J120)	Uxx-SLOT yy (J4)	CABLE	407273		
	BLK Aax RW 05 (J121)	Uxx-SLOT yy (J4)	CABLE	407273		

This system wirelist serves as a template for incorporating this harness assembly into the overall system wirelist. It does not in any way affect the fabrication of this harness assembly.

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DOCUMENT TI'I'LE	SIZE.	CODE NO	DOCUMENT NO.	REV
HARNESS ASSY, 1260-14,TTI	A	21793	407273	A
	DRN			SHEET 3 of 8

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ENGINEERING WIRE LIST

WIRE	FROM	TO	TYPE	PART #	WIRE LEN	REFERENCE
1	J100-1	J1-1	BRN	407250	41.5"	CHAN 01
2	J100-2	J1-2	TAN	407250	41.5"	CHAN 01 RTN
3	J100-3	J1-3	RED	407250	41.5"	CHAN 02
4	J100-4	J1-4	TAN	407250	41.5"	CHAN 02 RTN
5	J100-5	J1-5	ORN	407250	41.5"	CHAN 03
6	J100-6	J1-6	TAN	407250	41.5"	CHAN 03 RTN
7	JJ00-7	J1-7	YEL	407250	41.5"	CHAN 04
8	J100-8	J1-8	TAN	407250	41.5"	CHAN 04 RTN
9	J100-9	J1-9	GRN	407250	41.5"	CHAN 05
10	J100-10	J1-10	TAN	407250	41.5"	CHAN 05 RTN
11	J101-10	J1-11	BLU	407250	41.5"	CHAN 06
12	J101-9	J1-12	TAN	407250	41.5"	CHAN 06 RTN
13	J101-8	J1-13	VIO	407250	41.5"	CHAN 07
14	J101-7	J1-14	TAN	407250	41.5"	CHAN 07 RTN
15	J101-6	J1-15	GRY	407250	41.5"	CHAN 08
16	J101-5	J1-16	TAN	407250	41.5"	CHAN 08 RTN
17	J101-4	J1-17	WHT	407250	41.5"	CHAN 09
18	J101-3	J1-18	TAN	407250	41.5"	CHAN 09 RTN
19	J101-2	J1-19	BLK	407250	41.5"	CHAN 10
20	J101-1	J1-20	TAN	407250	41.5"	CHAN 10 RTN
21	J102-1	J1-21	BRN	407250	41.5"	CHAN 11
22	J102-2	J1-22	TAN	407250	41.5"	CHAN 11 RTN
23	J102-3	J1-23	RED	407250	41.5"	CHAN 12
24	J102-4	J1-24	TAN	407250	41.5"	CHAN 12 RTN
25	J102-5	J1-25	ORN	407250	41.5"	CHAN 13
26	J102-6	J1-26	TAN	407250	41.5"	CHAN 13 RTN
27	J102-7	J1-27	YEL	407250	41.5"	CHAN 14
28	J102-8	J1-28	TAN	407250	41.5"	CHAN 14 RTN
29	J102-9	J1-29	GRN	407250	41.5"	CHAN 15
30	J102-10	J1-30	TAN	407250	41.5"	CHAN 15 RTN
31	J103-10	J1-31	BLU	407250	41.5"	CHAN 16
32	J103-9	J1-32	TAN	407250	41.5"	CHAN 16 RTN
33	J103-8	J1-33	VIO	407250	41.5"	CHAN 17
34	J103-7	J1-34	TAN	407250	41.5"	CHAN 17 RTN
35	J103-6	J1-35	GRY	407250	41.5"	CHAN 18
36	J103-5	J1-36	TAN	407250	41.5"	CHAN 18 RTN
37	J103-4	J1-37	WHT	407250	41.5"	CHAN 19
38	J103-3	J1-38	TAN	407250	41.5"	CHAN 19 RTN
39	J103-2	J1-39	BLK	407250	41.5"	CHAN 20
40	J103-1	J1-40	TAN	407250	41.5"	CHAN 20 RTN
41	J104-1	J1-41	BRN	407250	41.5"	CHAN 21
42	J104-2	J1-42	TAN	407250	41.5"	CHAN 21 RTN
43	J104-3	J1-43	RED	407250	41.5"	CHAN 22
44	J104-4	J1-44	TAN	407250	41.5"	CHAN 22 RTN
45	J104-5	J1-45	ORN	407250	41.5"	CHAN 23
46	J104-6	J1-46	TAN	407250	41.5"	CHAN 23 RTN
47	J104-7	J1-47	YEL	407250	41.5"	CHAN 24
48	J104-8	J1-48	TAN	407250	41.5"	CHAN 24 RTN
49	J104-9	J1-49	GRN	407250	41.5"	BUSY
50	J104-10	J1-50	TAN	407250	41.5"	GND

RACAL Instruments, Inc., 4 Goodyear St., Irvine, CA 92718

DOCUMENT TI'LE	SIZE.	CODE NO	DOCUMENT NO.	REV
HARNESS ASSY, 1260-14,TTI	A	21793	407273	A
	DRN		SHEET 4 of 8	

ENGINEERING WIRE LIST

WIRE	FROM	TO	TYPE	PART #	WIRE LEN	REFERENCE
51	J105-1	J2-1	BRN	407250	41.5"	CHAN2S
52	J105-2	J2-2	TAN	407250	41.5"	CHAN 25 RTN
53	J105-3	J2-3	RED	407250	41.5"	CHAN 26
54	J105-4	J2-4	TAN	407250	41.5"	CHAN 26 RTN
55	J105-5	J2-5	ORN	407250	41.5"	CHAN 27
56	J105-6	J2-6	TAN	407250	41.5"	CHAN 27 RTN
57	J105-7	J2-7	YEL	407250	41.5"	CHAN 28
58	J105-8	J2-8	TAN	407250	41.5"	CHAN 28 RTN
59	J105-9	J2-9	GRN	407250	41.5"	CHAN 29
60	J105-10	J2-10	TAN	407250	41.5"	CHAN 29 RTN
61	J106-10	J2-11	BLU	407250	41.5"	CHAN 30
62	J106-9	J2-12	TAN	407250	41.5"	CHAN 30 RTN
63	J106-8	J2-13	VIO	407250	41.5"	CHAN 31
64	J106-7	J2-14	TAN	407250	41.5"	CHAN 31 RTN
65	J106-6	J2-15	GRY	407250	41.5"	CHAN 32
66	J106-5	J2-16	TAN	407250	41.5"	CHAN 32 RTN
67	J106-4	J2-17	WHT	407250	41.5"	CHAN 33
68	J106-3	J2-18	TAN	407250	41.5"	CHAN 33 RTN
69	J106-2	J2-19	BLK	407250	41.5"	CHAN 34
70	J106-1	J2-20	TAN	407250	41.5"	CHAN 34 RTN
71	J107-1	J2-21	BRN	407250	41.5"	CHAN 35
72	J107-2	J2-22	TAN	407250	41.5"	CHAN 35 RTN
73	J107-3	J2-23	RED	407250	41.5"	CHAN 36
74	J107-4	J2-24	TAN	407250	41.5"	CHAN 36 RTN
75	J107-5	J2-25	ORN	407250	41.5"	CHAN 37
76	J107-6	J2-26	TAN	407250	41.5"	CHAN 37 RTN
77	J107-7	J2-27	YEL	407250	41.5"	CHAN 38
78	J107-8	J2-28	TAN	407250	41.5"	CHAN 38 RTN
79	J107-9	J2-29	GRN	407250	41.5"	CHAN 39
80	J107-10	J2-30	TAN	407250	41.5"	CHAN 39 RTN
81	J108-10	J2-31	BLU	407250	41.5"	CHAN 40
82	J108-9	J2-32	TAN	407250	41.5"	CHAN 40 RTN
83	J108-8	J2-33	VIO	407250	41.5"	CHAN 41
84	J108-7	J2-34	TAN	407250	41.5"	CHAN 41 RTN
85	J108-6	J2-35	GRY	407250	41.5"	CHAN 42
86	J108-5	J2-36	TAN	407250	41.5"	CHAN 42 RTN
87	J108-4	J2-37	WHT	407250	41.5"	CHAN 43
88	J108-3	J2-38	TAN	407250	41.5"	CHAN 43 RTN
89	J108-2	J2-39	BLK	407250	41.5"	CHAN 44
90	J108-1	J2-40	TAN	407250	41.5"	CHAN 44 RTN
91	J109-1	J2-41	BRN	407250	41.5"	CHAN 45
92	J109-2	J2-42	TAN	407250	41.5"	CHAN 45 RTN
93	J109-3	J2-43	RED	407250	41.5"	CHAN 46
94	J109-4	J2-44	TAN	407250	41.5"	CHAN 46 RTN
95	J109-5	J2-45	ORN	407250	41.5"	CHAN 47
96	J109-6	J2-46	TAN	407250	41.5'	CHAN 47 RTN
97	J109-7	J2-47	YEL	407250	41.5"	CHAN 48
98	J109-8	J2-48	TAN	407250	41.5"	CHAN 48 RTN

RACAL Instruments, Inc., 4 Goodyear St., Irvine, CA 92718

DOCUMENT TI'I'LE	SIZE.	CODE NO	DOCUMENT NO.	REV
HARNESS ASSY, 1260-14,TTI	A	21793	407273	A
	DRN			SHEET 5 of 8

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ENGINEERING WIRE LIST

WIRE	FROM	TO	TYPE	PART #	WIRE LEN	REFERENCE
99	J109-9	J2-49	ORN	407250	41.5"	CLOCK IN
100	J109-10	J2-50	TAN	407250	41.5"	CLOCK IN RTN
101	J110-1	J3-1	BRN	407255	41.5"	CHAN 49
102	J110-2	J3-2	TAN	407255	41.5"	CHAN 49 RTN
103	J110-3	J3-3	RED	407255	41.5"	CHAN 50
104	J110-4	J3-4	TAN	407255	41.5"	CHAN 50 RTN
105	J110-5	J3-5	ORN	407255	41.5"	CHAN 51
106	J110-6	J3-6	TAN	407255	41.5"	CHAN 51 RTN
107	J110-7	J3-7	YEL	407255	41.5"	CHAN 52
108	J110-8	J3-8	TAN	407255	41.5"	CHAN 52 RTN
109	J110-9	J3-9	GRN	407255	41.5"	CHAN 53
110	J110-10	J3-10	TAN	407255	41.5"	CHAN 53 RTN
111	J111-10	J3-11	BLU	407255	41.5"	CHAN 54
112	J111-9	J3-12	TAN	407255	41.5"	CHAN 54 RTN
113	J111-8	J3-13	VIO	407255	41.5"	CHAN 55
114	J111-7	J3-14	TAN	407255	41.5"	CHAN 55 RTN
115	J111-6	J3-15	GRY	407255	41.5"	CHAN 56
116	J111-5	J3-16	TAN	407255	41.5"	CHAN 56 RTN
117	J111-4	J3-17	WHT	407255	41.5"	CHAN 57
118	J111-3	J3-18	TAN	407255	41.5"	CHAN 57 RTN
119	J111-2	J3-19	BLK	407255	41.5"	CHAN 58
120	J111-1	J3-20	TAN	407255	41.5"	CHAN 58 RTN
121	J112-1	J3-21	BRN	407255	41.5"	CHAN 59
122	J112-2	J3-22	TAN	407255	41.5"	CHAN 59 RTN
123	J112-3	J3-23	RED	407255	41.5"	CHAN 60
124	J112-4	J3-24	TAN	407255	41.5"	CHAN 60 RTN
125	J112-5	J3-25	ORN	407255	41.5"	CHAN 61
126	J112-6	J3-26	TAN	407255	41.5"	CHAN 61 RTN
127	J112-7	J3-27	YEL	407255	41.5"	CHAN 62
128	J112-8	J3-28	TAN	407255	41.5"	CHAN 62 RTN
129	J112-9	J3-29	GRN	407255	41.5"	CHAN 63
130	J112-10	J3-30	TAN	407255	41.5"	CHAN 63 RTN
131	J113-10	J3-31	BLU	407255	41.5"	CHAN 64
132	J113-9	J3-32	TAN	407255	41.5"	CHAN 64 RTN
133	J113-8	J3-33	VIO	407255	41.5"	CHAN 65
134	J113-7	J3-34	TAN	407255	41.5"	CHAN 65 RTN
135	J113-6	J3-35	GRY	407255	41.5"	CHAN 66
136	J113-5	J3-36	TAN	407255	41.5"	CHAN 66 RTN
137	J113-4	J3-37	WHT	407255	41.5"	CHAN 67
138	J113-3	J3-38	TAN	407255	41.5"	CHAN 67 RTN
139	J113-2	J3-39	BLK	407255	41.5"	CHAN 68
140	J113-1	J3-40	TAN	407255	41.5"	CHAN 68 RTN
141	J114-1	J3-41	BRN	407255	41.5"	CHAN 69
142	J114-2	J3-42	TAN	407255	41.5"	CHAN 69 RTN
143	J114-3	J3-43	RED	407255	41.5"	CHAN 70
144	J114-4	J3-44	TAN	407255	41.5"	CHAN 70 RTN
145	J114-5	J3-45	ORN	407255	41.5"	CHAN 7I
146	J114-6	J3-46	TAN	407255	41.5"	CHAN 71 RTN

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HARNESS ASSY, 1260-14,TTI	A	21793	407273	A
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ENGINEERING WIRE LIST

WIRE	FROM	TO	TYPE	PART #	WIRE LEN	REFERENCE
147	J114-7	J3-47	YEL	407255	41.5"	CHAN 72
148	J114-8	J3-48	TAN	407255	41.5"	CHAN 72 RTN
149	J114-9	J3-49	GRN	407255	41.5"	EDRVR 00
150	J114-10	J3-50	TAN	407255	41.5"	EDRVR 00 RTN
151	J115-10	J3-51	BLU	407255	41.5"	EDRVR 01
152	J115-9	J3-52	TAN	407255	41.5"	EDRVR 01 RTN
153	J115-8	J3-53	VIO	407255	41.5"	EDRVR 02
154	J115-7	J3-54	TAN	407255	41.5"	EDRVR 02 RTN
155	J115-6	J3-55	GRY	407255	41.5"	EDRVR 03
156	J115-5	J3-56	TAN	407255	41.5"	EDRVR 03 RTN
157	J115-4	J3-57	WHT	407255	41.5"	EDRVR 04
158	J115-3	J3-58	TAN	407255	41.5"	EDRVR 04 RTN
159	J115-2	J3-59	BLK	407255	41.5"	EDRVR 05
160	J115-1	J3-60	TAN	407255	41.5"	EDRVR 05 RTN
161	J116-1	J4-1	BRN	407255	41.5"	CHAN 73
162	J116-2	J4-2	TAN	407255	41.5"	CHAN 73 RTN
163	J116-3	J4-3	RED	407255	41.5"	CHAN 74
164	J116-4	J4-4	TAN	407255	41.5"	CHAN 74 RTN
165	J116-5	J4-5	ORN	407255	41.5"	CHAN 75
166	J116-6	J4-6	TAN	407255	41.5"	CHAN 75 RTN
167	J116-7	J4-7	YEL	407255	41.5"	CHAN 76
168	J116-8	J4-8	TAN	407255	41.5"	CHAN 76 RTN
169	J116-9	J4-9	GRN	407255	41.5"	CHAN 77
170	J116-10	J4-10	TAN	407255	41.5"	CHAN 77 RTN
171	J117-10	J4-11	BLU	407255	41.5"	CHAN 78
172	J117-9	J4-12	TAN	407255	41.5"	CHAN 78 RTN
173	J117-8	J4-13	VIO	407255	41.5"	CHAN 79
174	J117-7	J4-14	TAN	407255	41.5"	CHAN 79 RTN
175	J117-6	J4-15	GRY	407255	41.5"	CHAN 80
176	J117-5	J4-16	TAN	407255	41.5"	CHAN 80 RTN
177	J117-4	J4-17	WHT	407255	41.5"	CHAN 81
178	J117-3	J4-18	TAN	407255	41.5"	CHAN 81 RTN
179	J117-2	J4-19	BLK	407255	41.5"	CHAN 82
180	J117-1	J4-20	TAN	407255	41.5"	CHAN 82 RTN
181	J118-1	J4-21	BRN	407255	41.5"	CIIAN 83
182	J118-2	J4-22	TAN	407255	41.5"	CHAN 83 RTN
183	J118-3	J4-23	RED	407255	41.5"	CHAN 84
184	J118-4	J4-24	TAN	407255	41.5"	CHAN 84 RTN
185	J118-5	J4-25	ORN	407255	41.5"	CHAN 85
186	J118-6	J4-26	TAN	407255	41.5"	CHAN 85 RTN
187	J118-7	J4-27	YEL	407255	41.5"	CHAN 86
188	J118-8	J4-28	TAN	407255	41.5"	CHAN 86 RTN
189	J118-9	J4-29	GRN	407255	41.5"	CHAN 87
190	J118-10	J4-30	TAN	407255	41.5"	CHAN 87 RTN
191	J119-10	J4-31	BLU	407255	41.5"	CHAN 88
192	J119-9	J4-32	TAN	407255	41.5"	CHAN 88 RTN
193	J119-8	J4-33	VIO	407255	41.5"	CHAN 89
194	J119-7	J4-34	TAN	407255	41.5"	CHAN 89 RTN

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ENGINEERING WIRE LIST

WIRE	FROM	TO	TYPE	PART #	WIRE LEN	REFERENCE
195	J119-6	J4-35	GRY	407255	41.5″	CHAN 90
196	J119-5	J4-36	TAN	407255	41.5"	CHAN 90 RTN
197	J119-4	J4-37	WHT	407255	41.5"	CHAN 91
198	J119-3	J4-38	TAN	407255	41.5"	CHAN 91 RTN
199	J119-2	J4-39	BLK	407255	41.5"	CHAN 92
200	J119-1	J4-40	TAN	407255	41.5"	CHAN 92 RTN
201	J120-1	J4-41	BRN	407255	41.5"	CHAN 93
202	J120-2	J4-42	TAN	407255	41.5"	CHAN 93 RTN
203	J120-3	J4-43	RED	407255	41.5"	CHAN 94
204	J120-4	J4-44	TAN	407255	41.5"	CHAN 94 RTN
205	J120-5	J4-45	ORN	407255	41.5"	CHAN 95
206	J120-6	J4-46	TAN	407255	41.5"	CHAN 95 RTN
207	J120-7	J4-47	YEL	407255	41.5"	CHAN 96
208	J120-8	J4-48	TAN	407255	41.5"	CHAN 96 RTN
209	J120-9	J4-49	GRN	407255	41.5"	EDRYR 06
210	J120-10	J4-50	TAN	407255	41.5"	EDRVR 06 RTN
211	J121-10	J4-51	BLU	407255	41.5"	EDRVR 07
212	J121-9	J4-52	TAN	407255	41.5"	EDRVR 07 RTN
213	J121-8	J4-53	VIO	407255	41.5"	EDRVR 08
214	J121-7	J4-54	TAN	407255	41.5"	EDRVR 08 RTN
215	J121-6	J4-55	GRY	407255	41.5"	EDRVR 09
216	J121-5	J4-56	TAN	407255	41.5"	EDRVR 09 RTN
217	J121-4	J4-57	WHT	407255	41.5"	EDRYR 10
218	J121-3	J4-58	TAN	407255	41.5"	EDRVR 10 RTN
219	J121-2	J4-59	BLK	407255	41.5"	EDRVR 11
220	J121-1	J4-60	TAN	407255	41.5"	EDRVR 11 RTN

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DOCUMENT TI'LE	SIZE.	CODE NO	DOCUMENT NO.	REV
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Chapter 5
PRODUCT SUPPORT

Product Support

EADS North America Defense Test and Services, Inc. has a complete Service and Parts Department. If you need technical assistance or should it be necessary to return your product for repair or calibration, call 1-800-722-3262. If parts are required to repair the product at your facility, call 1-949-859-8999 and ask for the Parts Department.

When sending your instrument in for repair, complete the form in the back of this manual.

For worldwide support and the office closest to your facility, refer to the website for the most complete information http://www.eads-nadefense.com.

Warranty

Use the original packing material when returning the 1260-14 to EADS North America Defense Test and Services, Inc. for calibration or servicing. The original shipping container and associated packaging material will provide the necessary protection for safe reshipment.

If the original packing material is unavailable, contact EADS North America Defense Test and Services, Inc. Customer Service at 1-800-722-3262 for information.

REPAIR AND CALIBRATION REQUEST FORM

To allow us to better understand your repair requests, we suggest you use the following outline when calling and include a copy with your instrument to be sent to the EADS North America Defense Test and Service, Inc. Repair Facility.

Model_____ Serial No._____ Date_____

Company Name_____ Purchase Order #_____

Billing Address_____

City

State/Province Zip/Postal Code Country

Shipping Address_____

City

State/Province Zip/Postal Code Country

Technical Contact_____ Phone Number ( )_____
Purchasing Contact_____ Phone Number ( )_____

1. Describe, in detail, the problem and symptoms you are having. Please include all set up details, such as input/output levels, frequencies, waveform details, etc.

2. If problem is occurring when unit is in remote, please list the program strings used and the controller type.

3. Please give any additional information you feel would be beneficial in facilitating a faster repair time (i.e., modifications, etc.)

4. Is calibration data required? Yes No (please circle one)

Call before shipping
Note: We do not accept "collect" shipments.

Ship instruments to nearest support office.

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